

FIG. 1

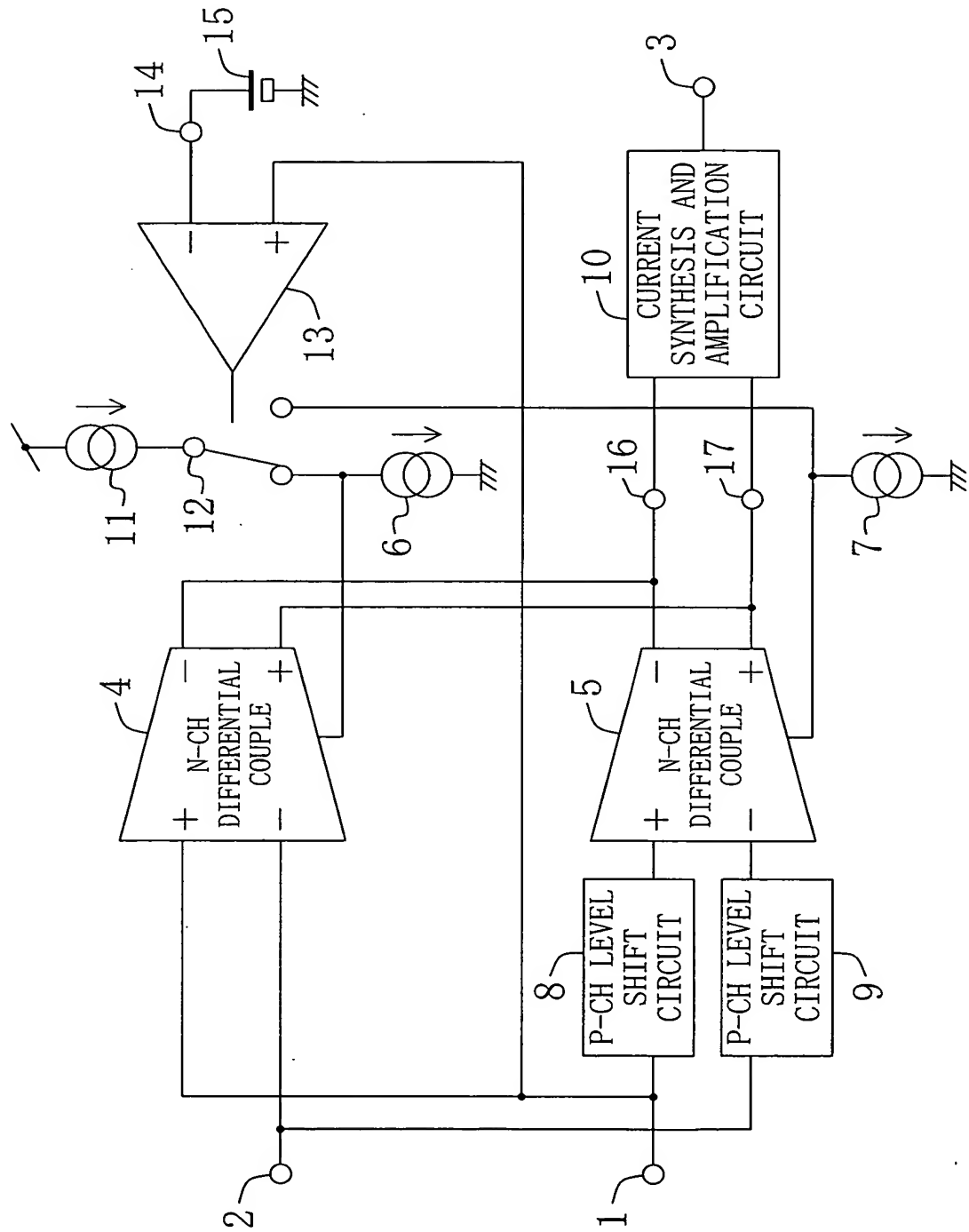


FIG. 2

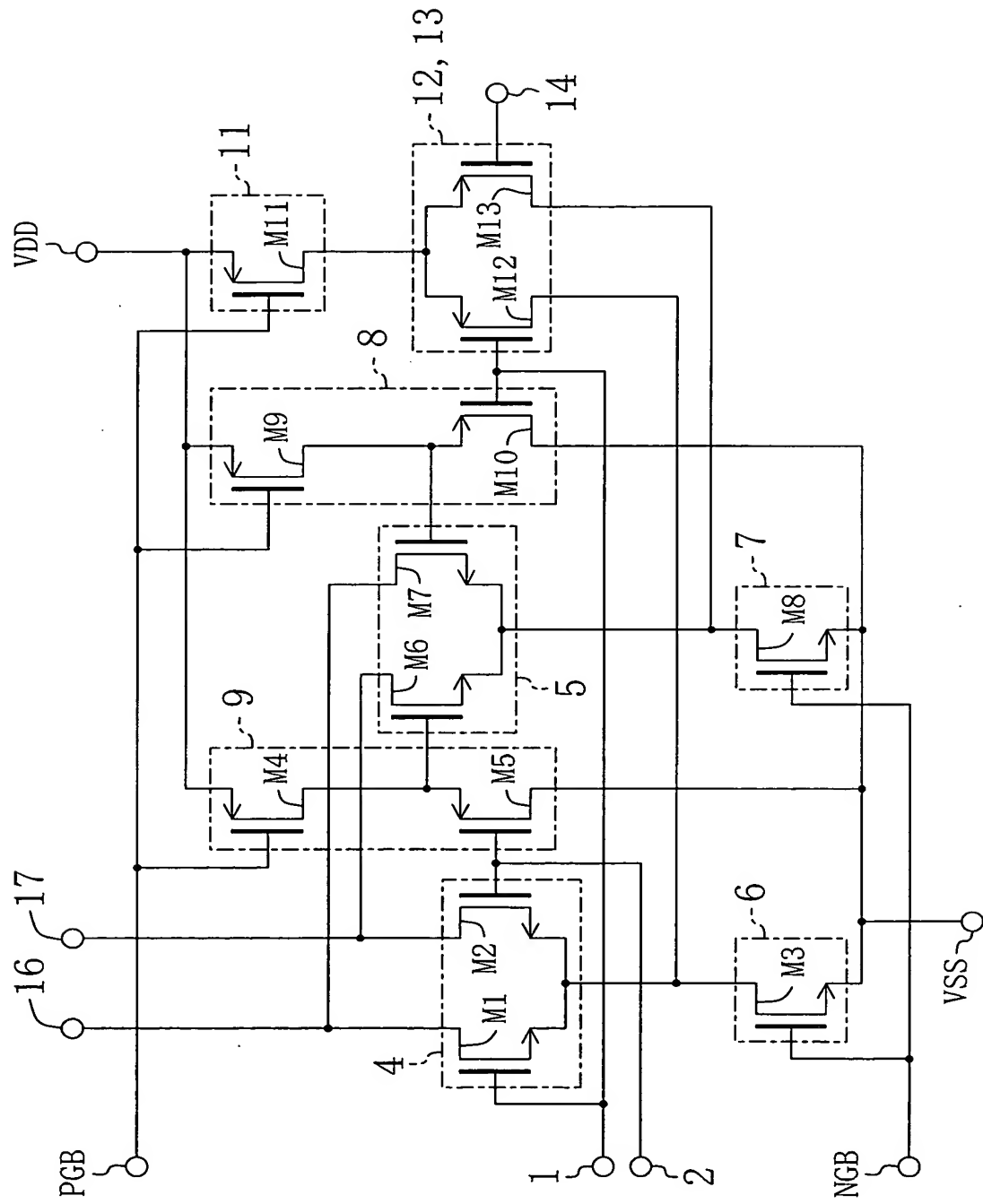


FIG. 3

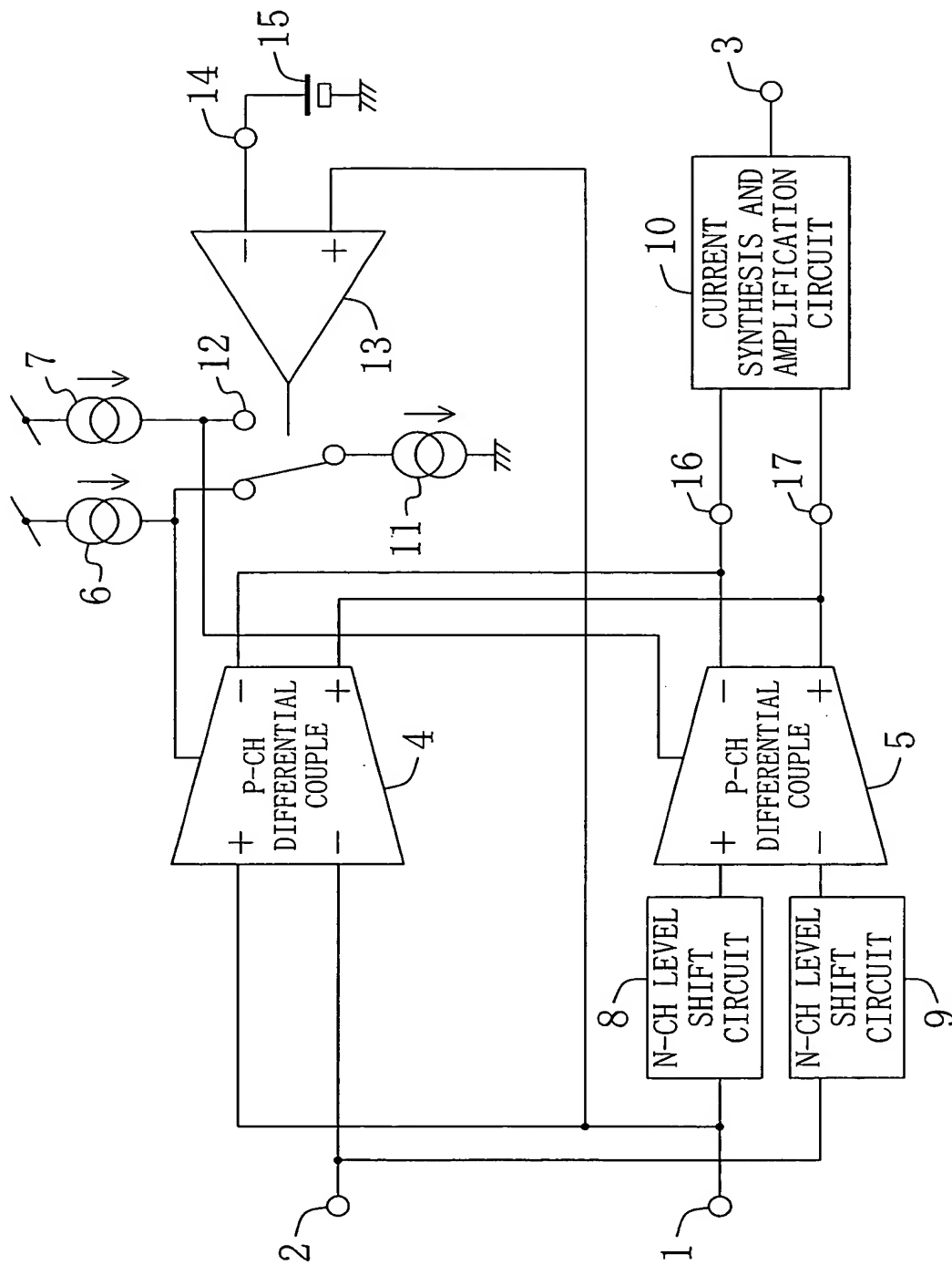


FIG. 4

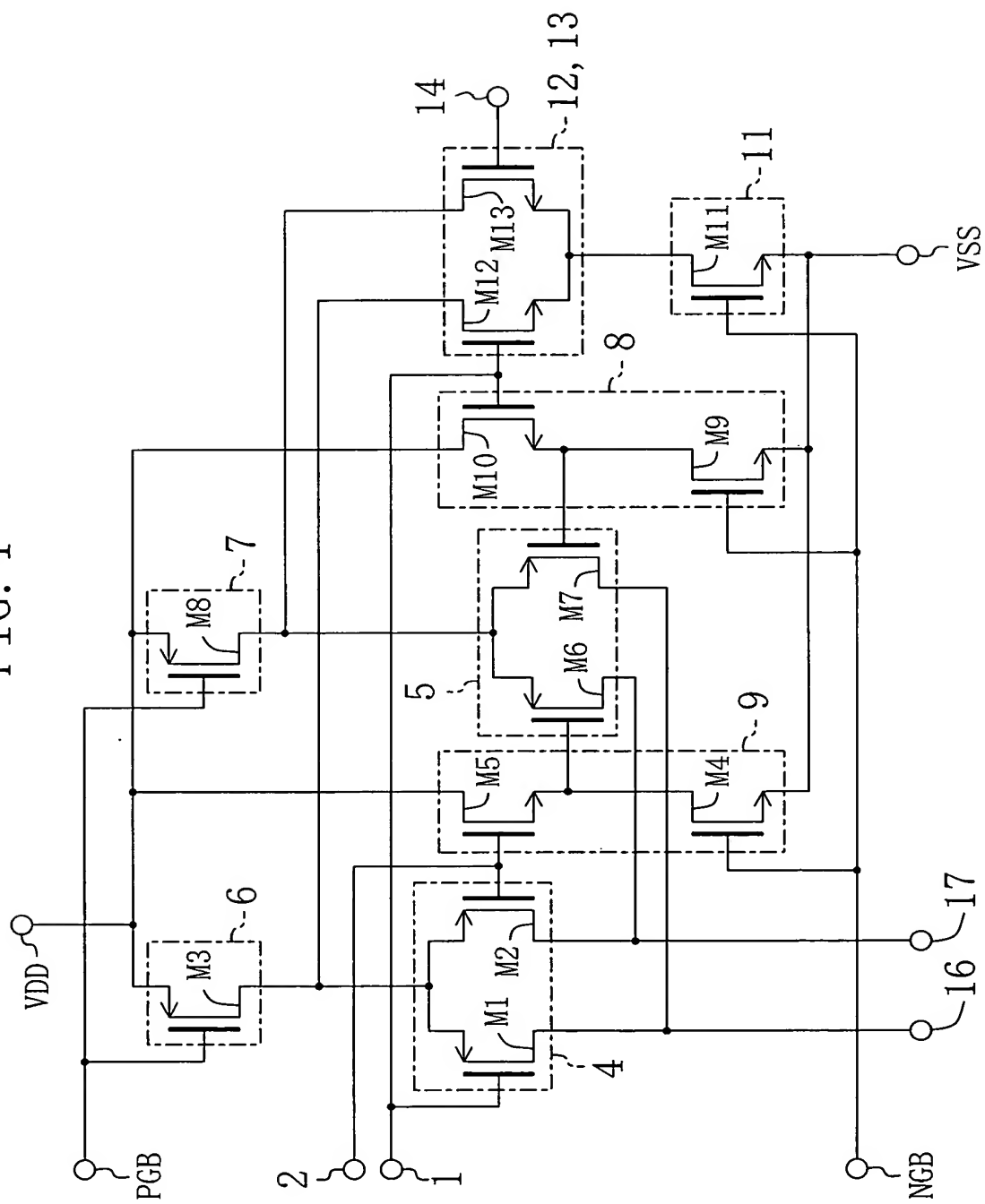


FIG. 5

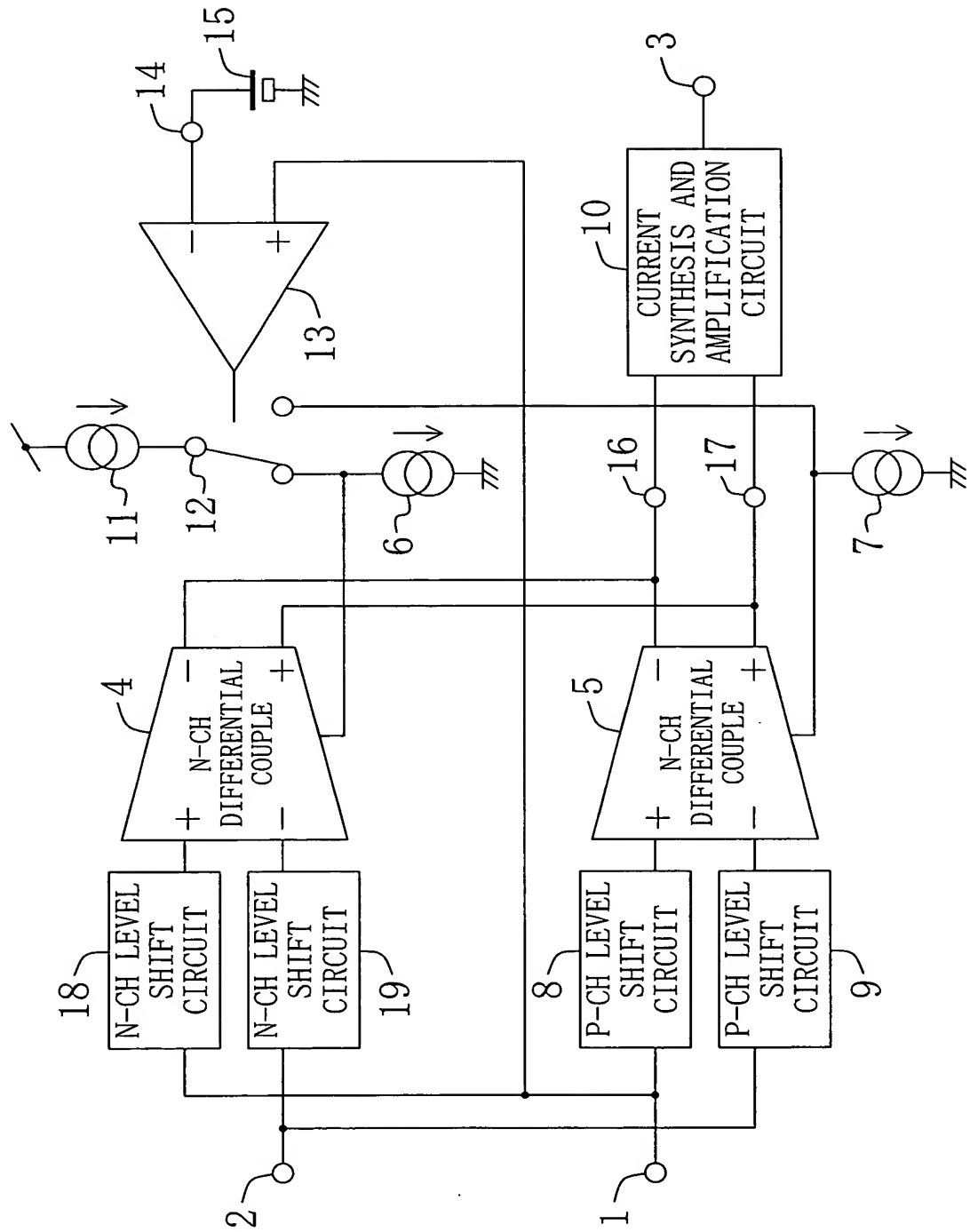


FIG. 6

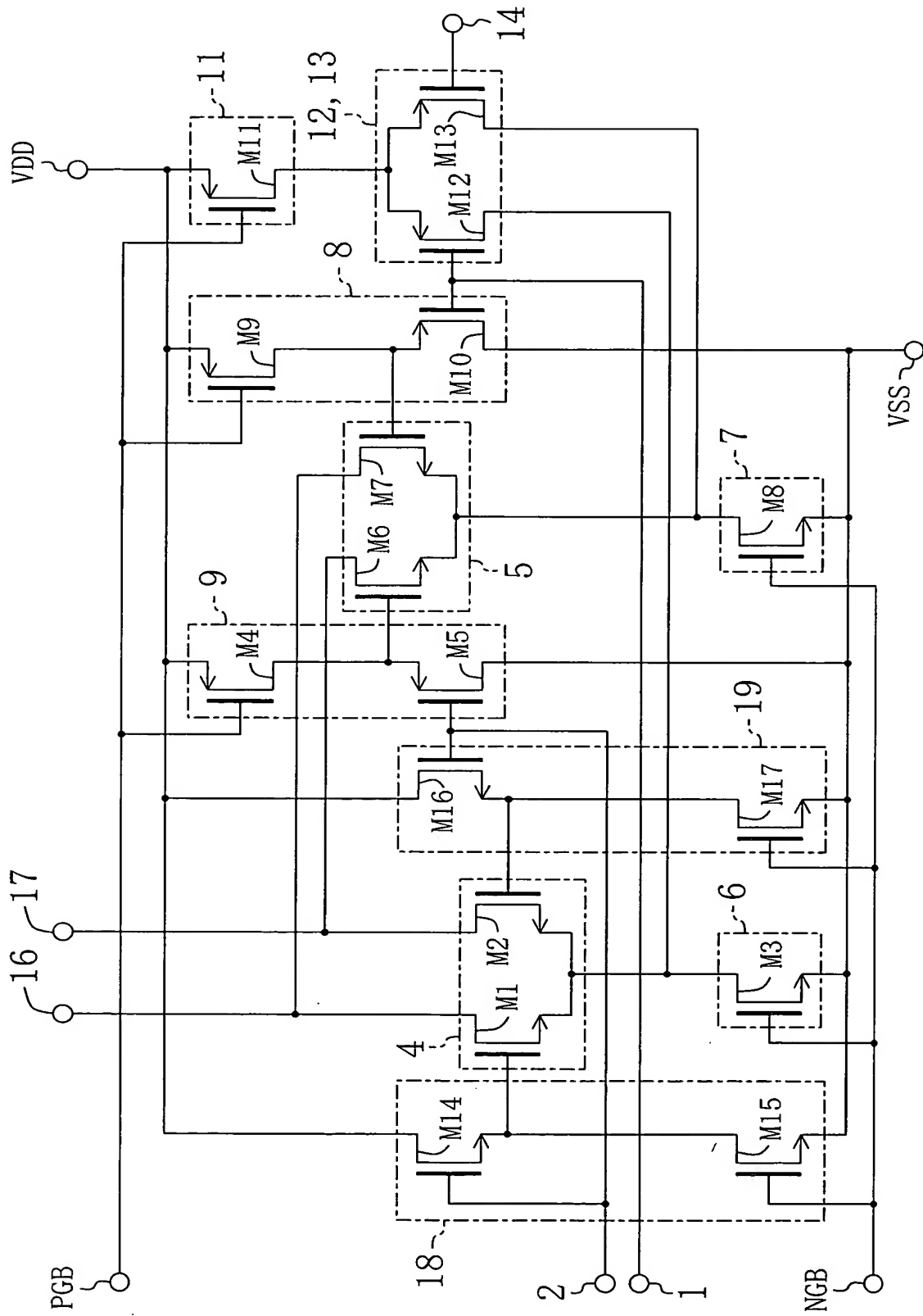


FIG. 7

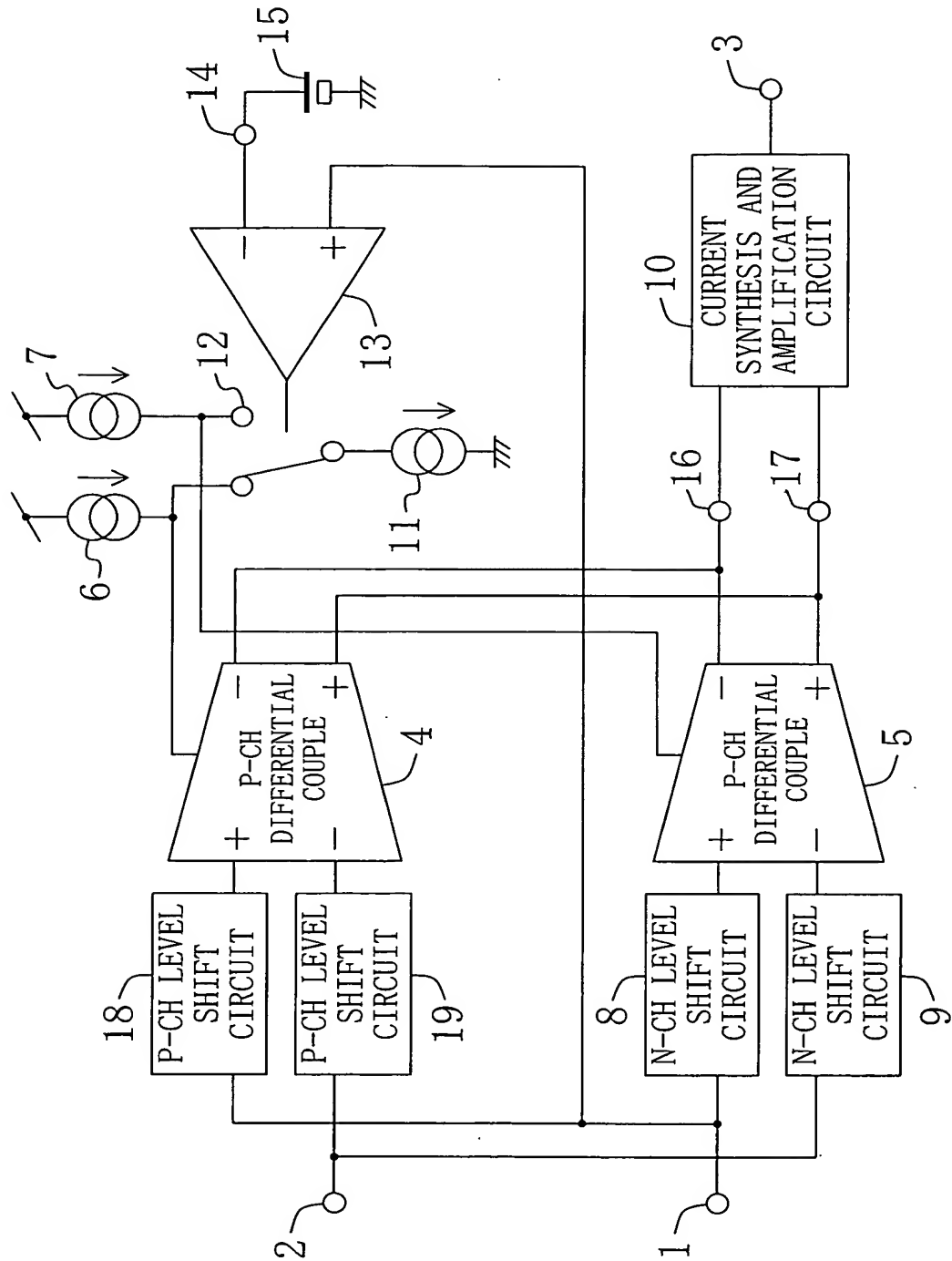


FIG. 8

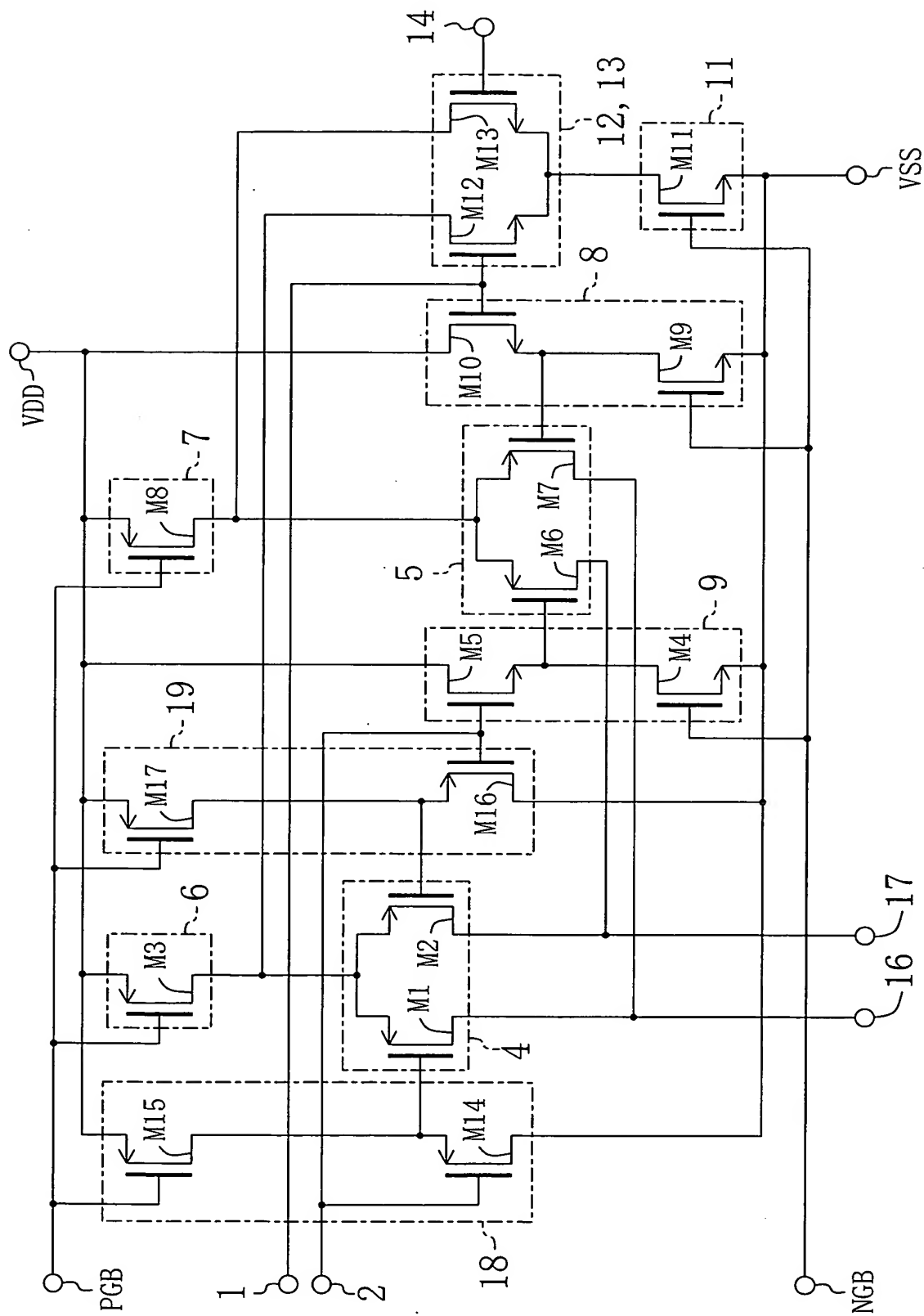




FIG. 9

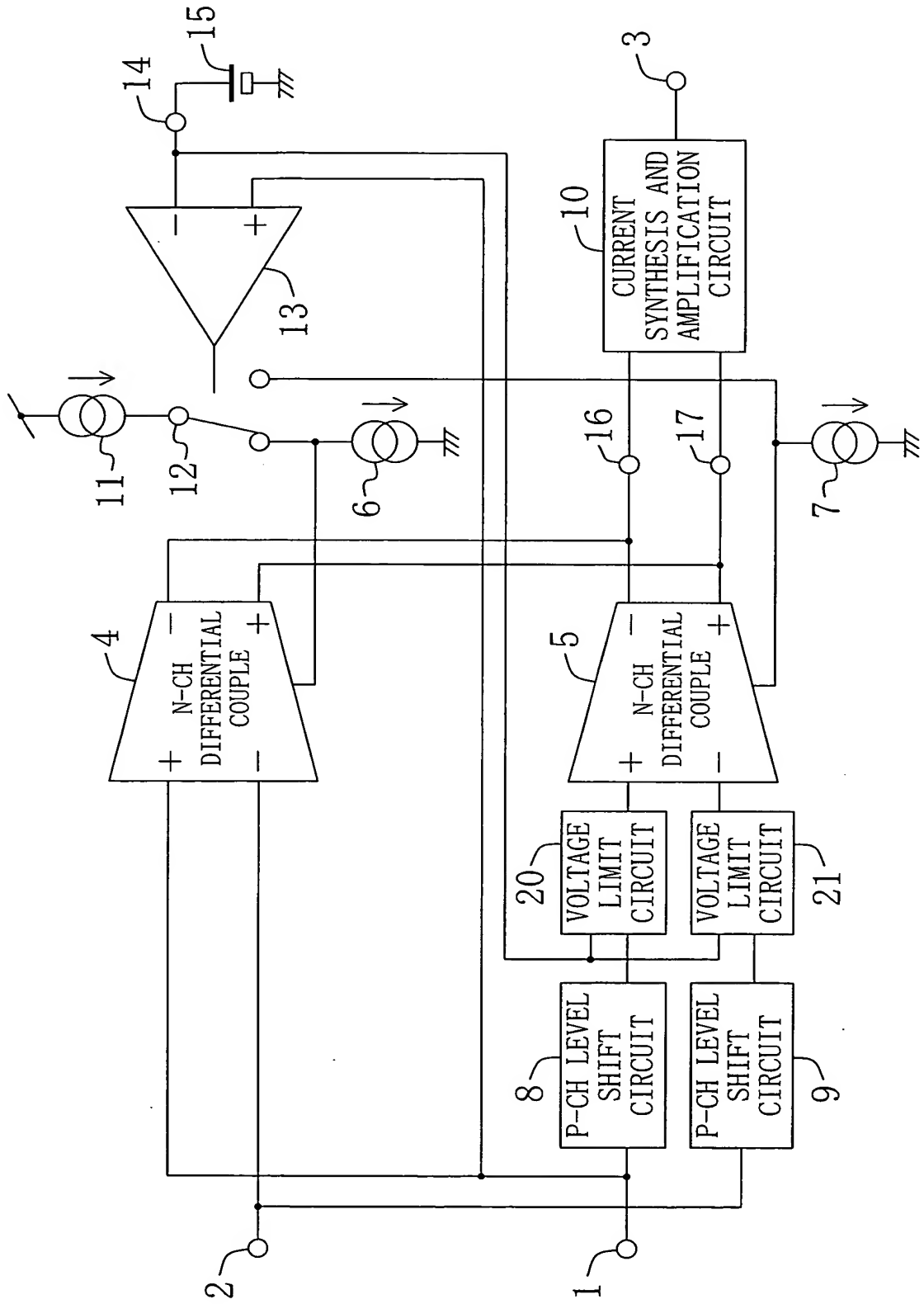


FIG. 10

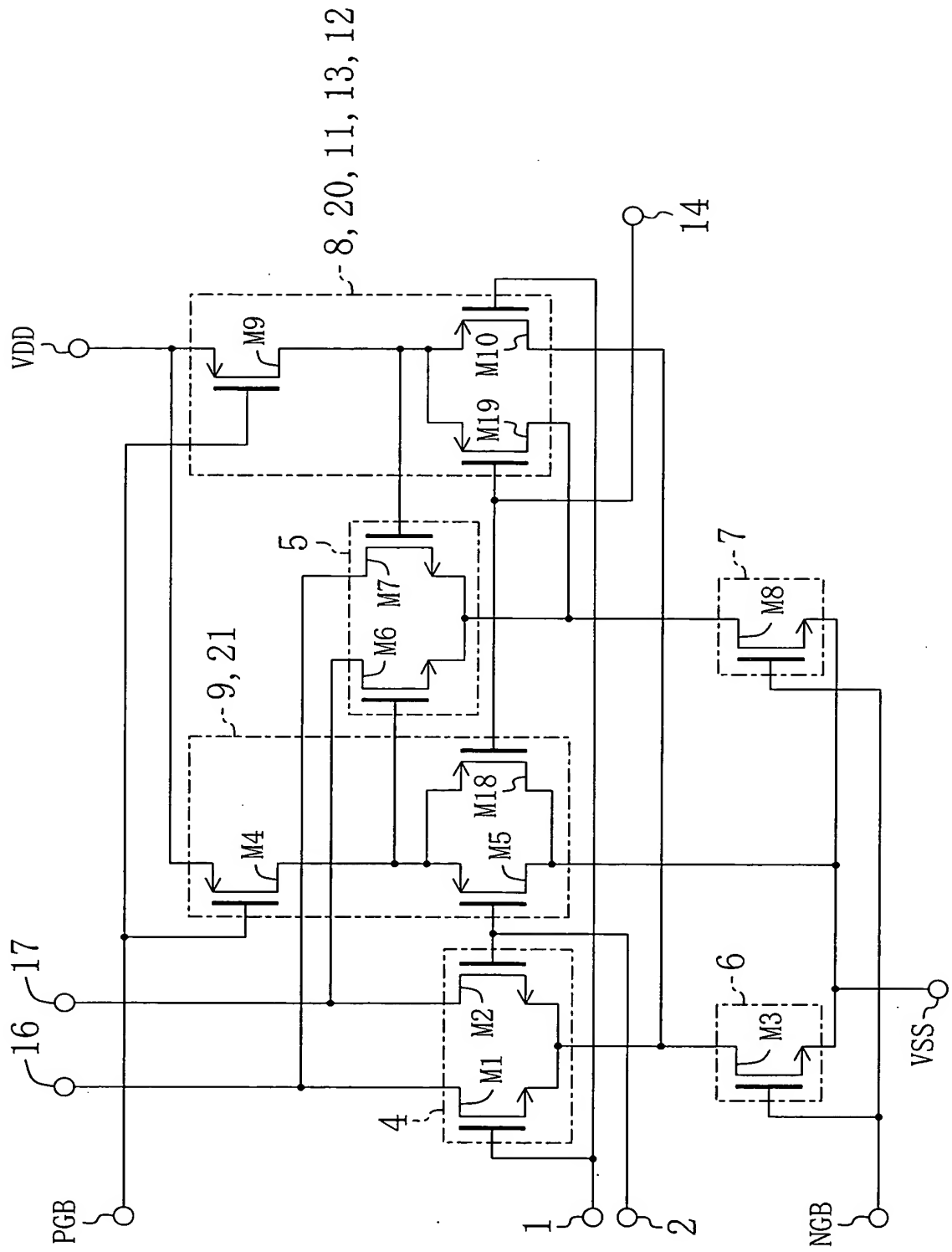


FIG. 11

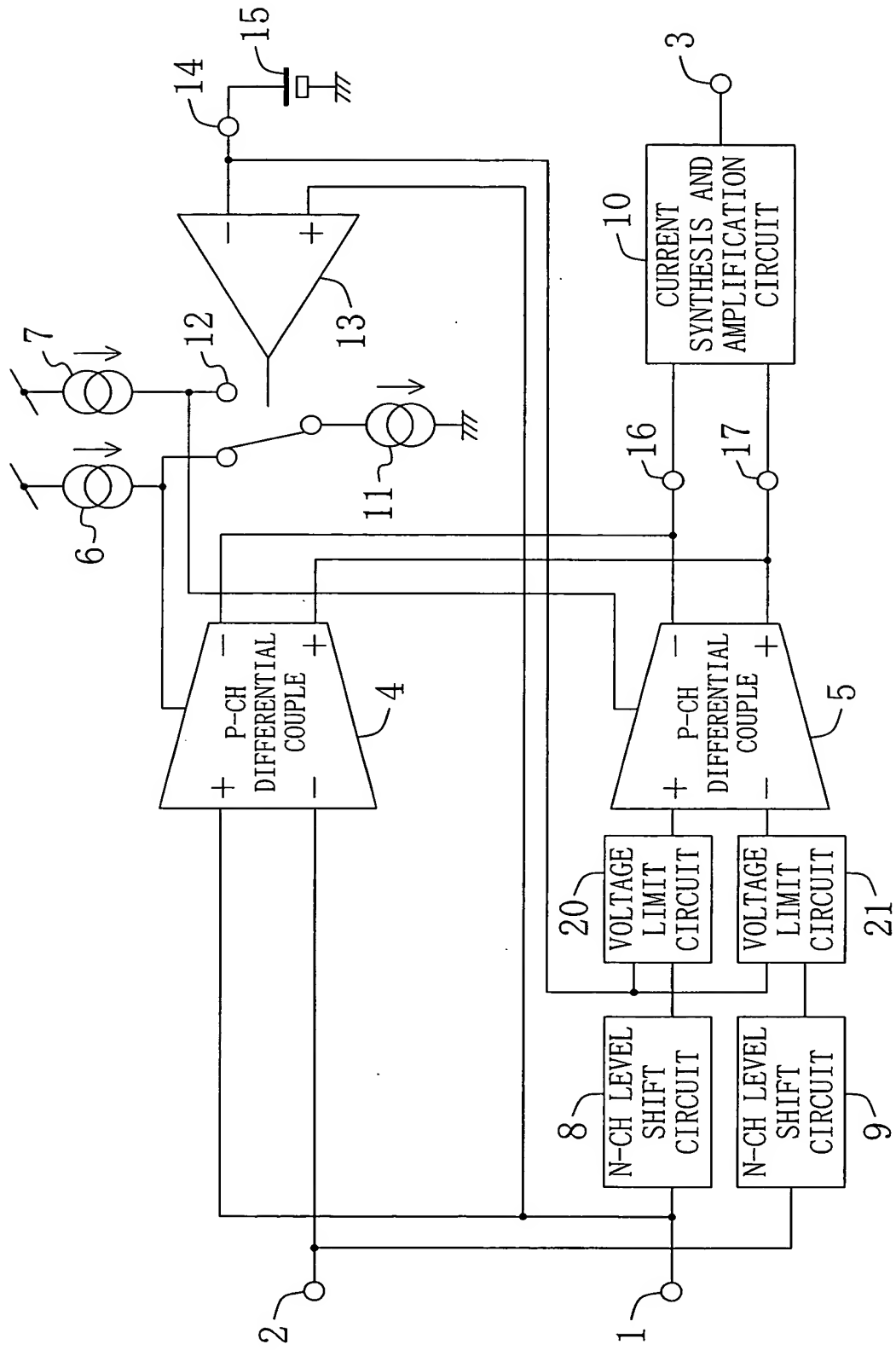


FIG. 12

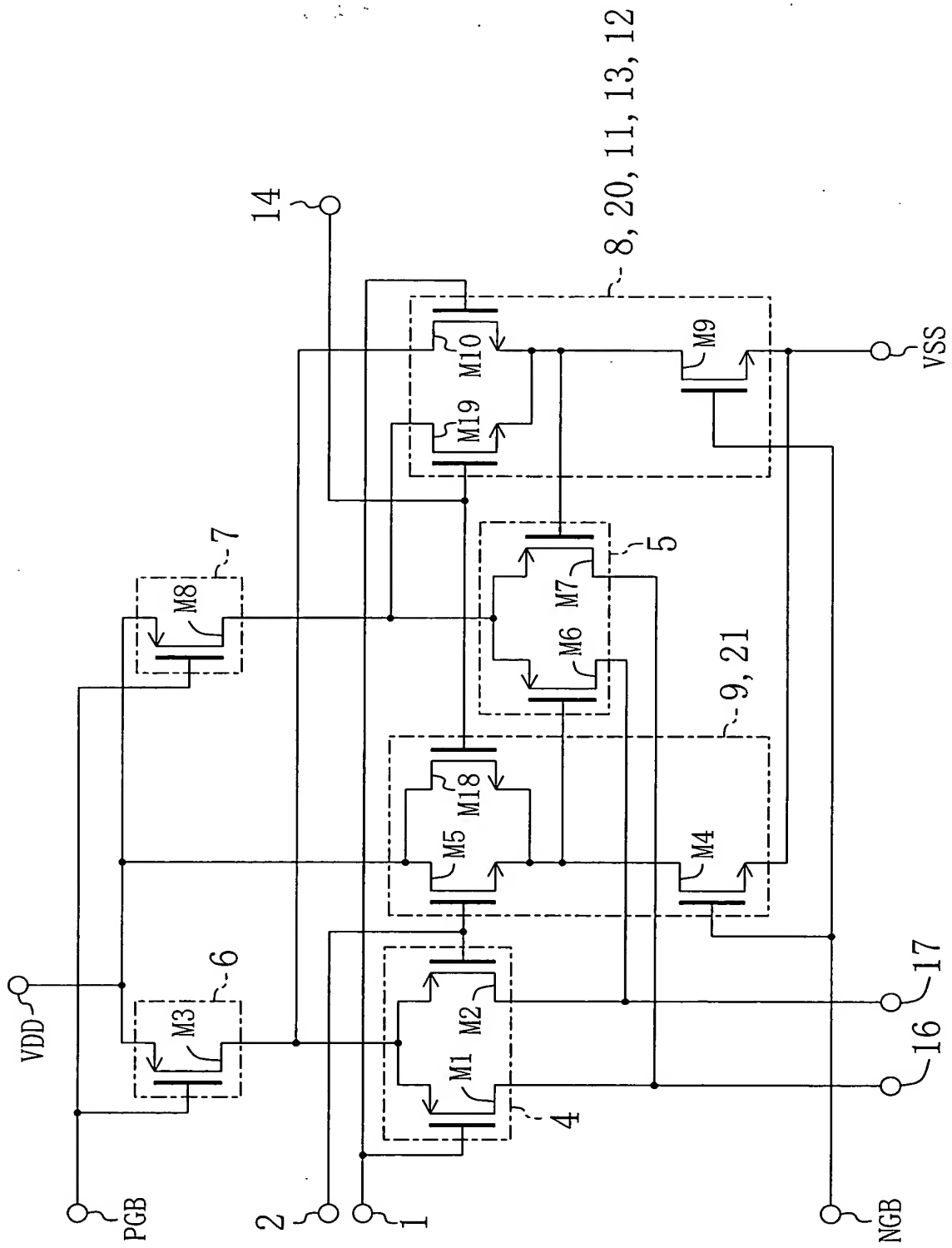


FIG. 13

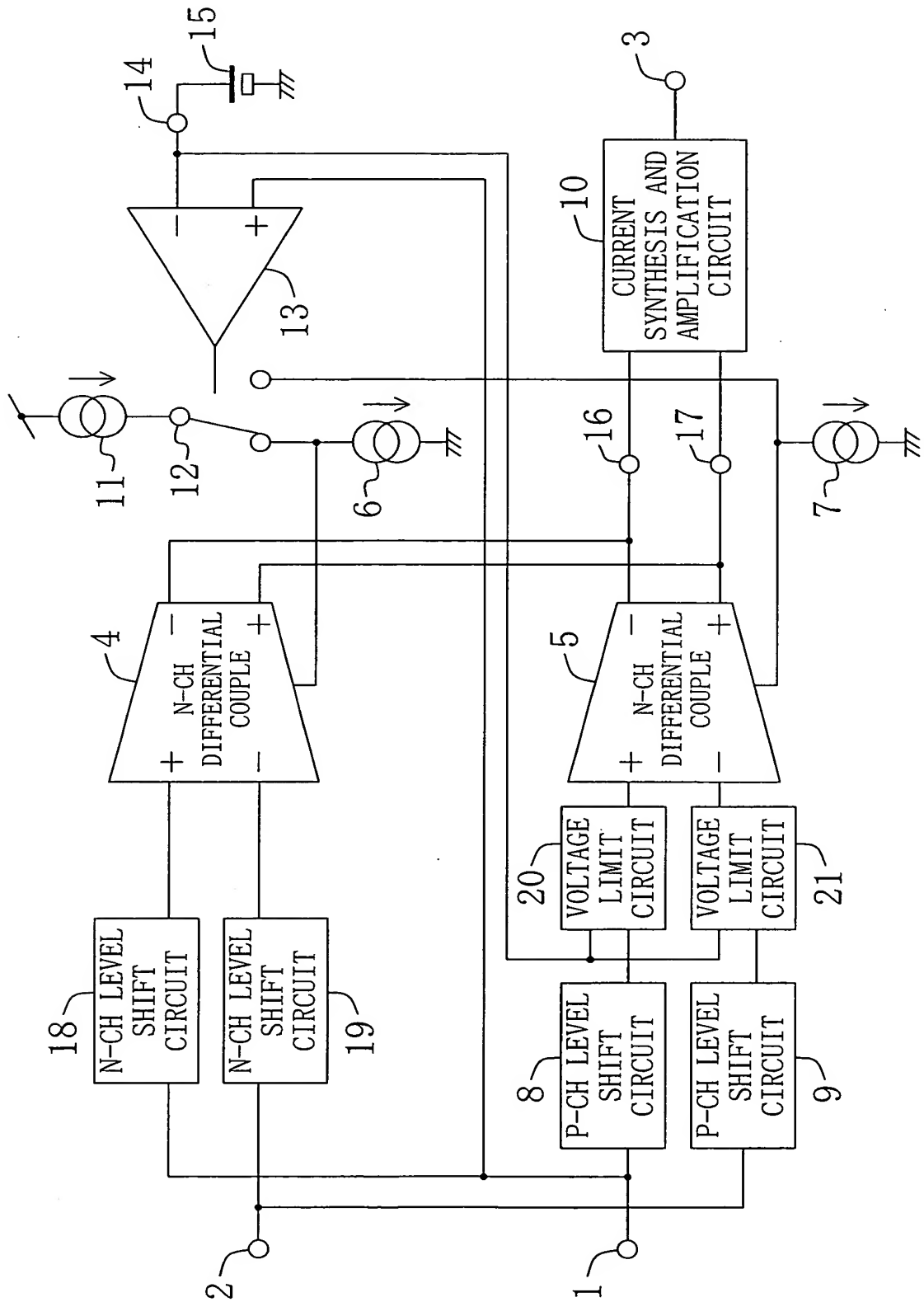


FIG. 14

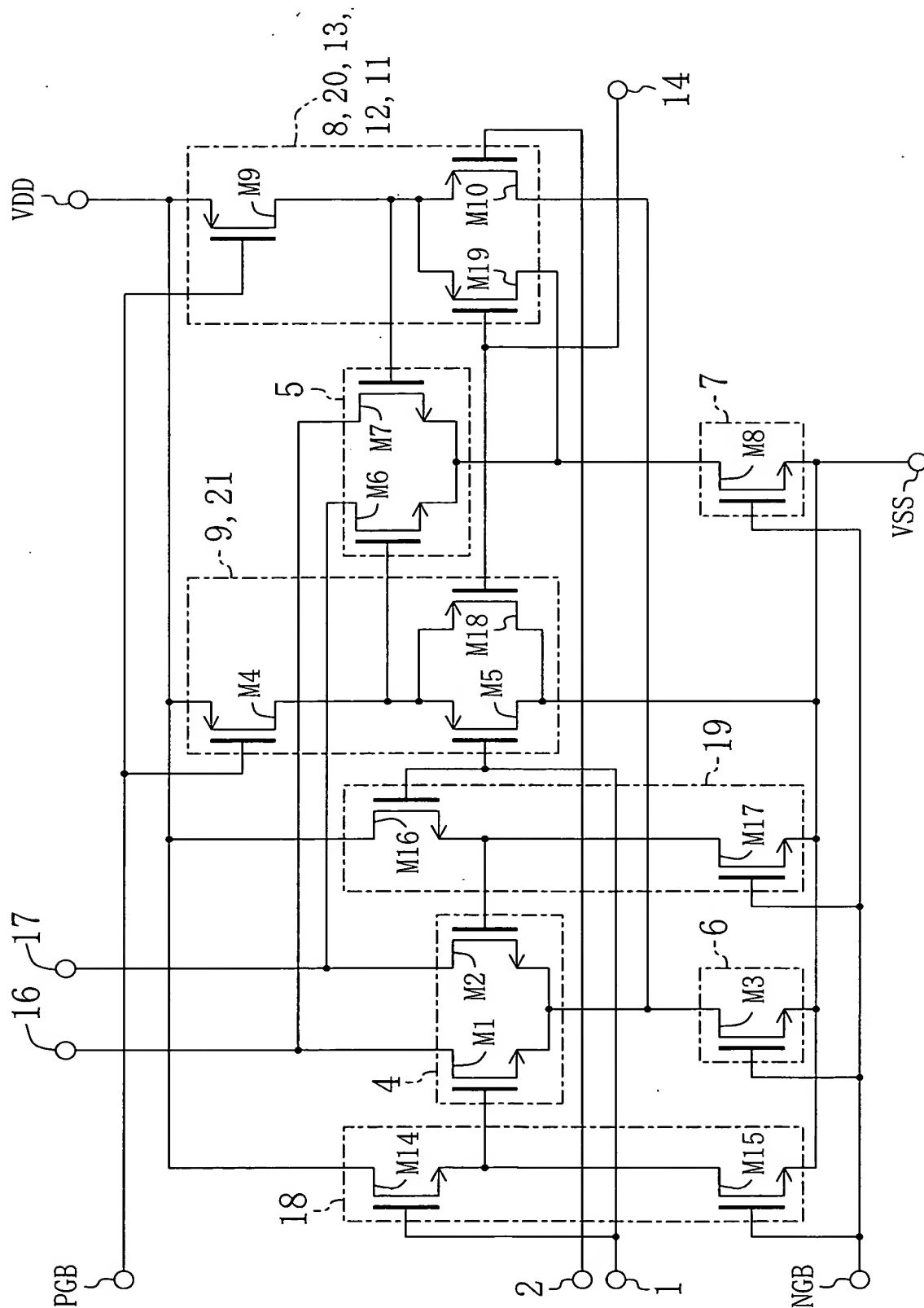
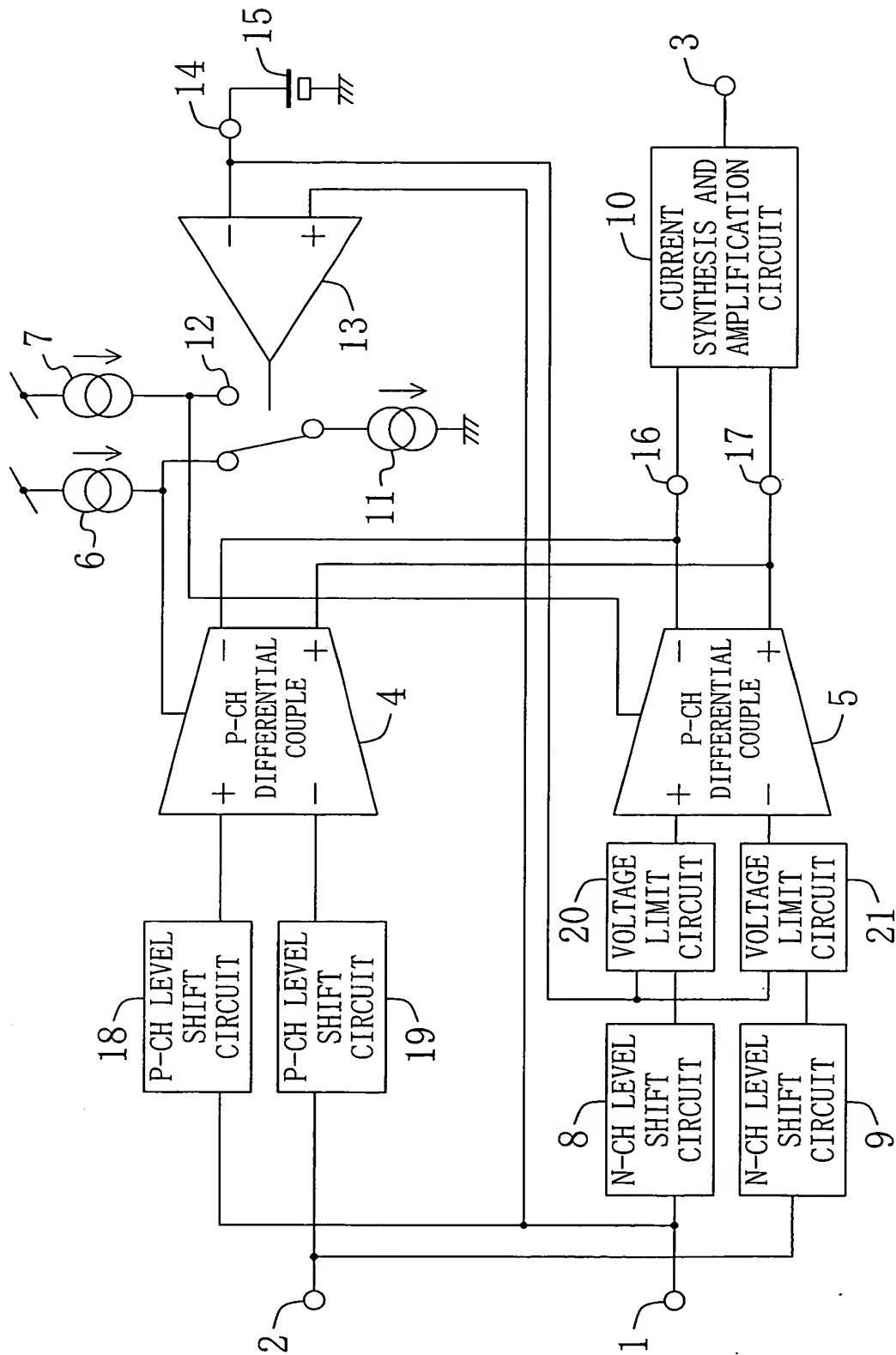


FIG. 15



The circuit diagram illustrates a 1T1C1D1E1S1P1 circuit. It features 21 transistors (M1-M21) and 14 nodes (1-14). The circuit is powered by VSS and VDD. The input is connected to node 1, and the output is connected to node 14. The circuit includes a PMOS network (M1-M10) and an NMOS network (M11-M21). The PMOS network is connected to VDD, and the NMOS network is connected to VSS. The circuit is designed to implement a specific logic function, with the output node 14 being the result of the logic operation.



FIG. 17

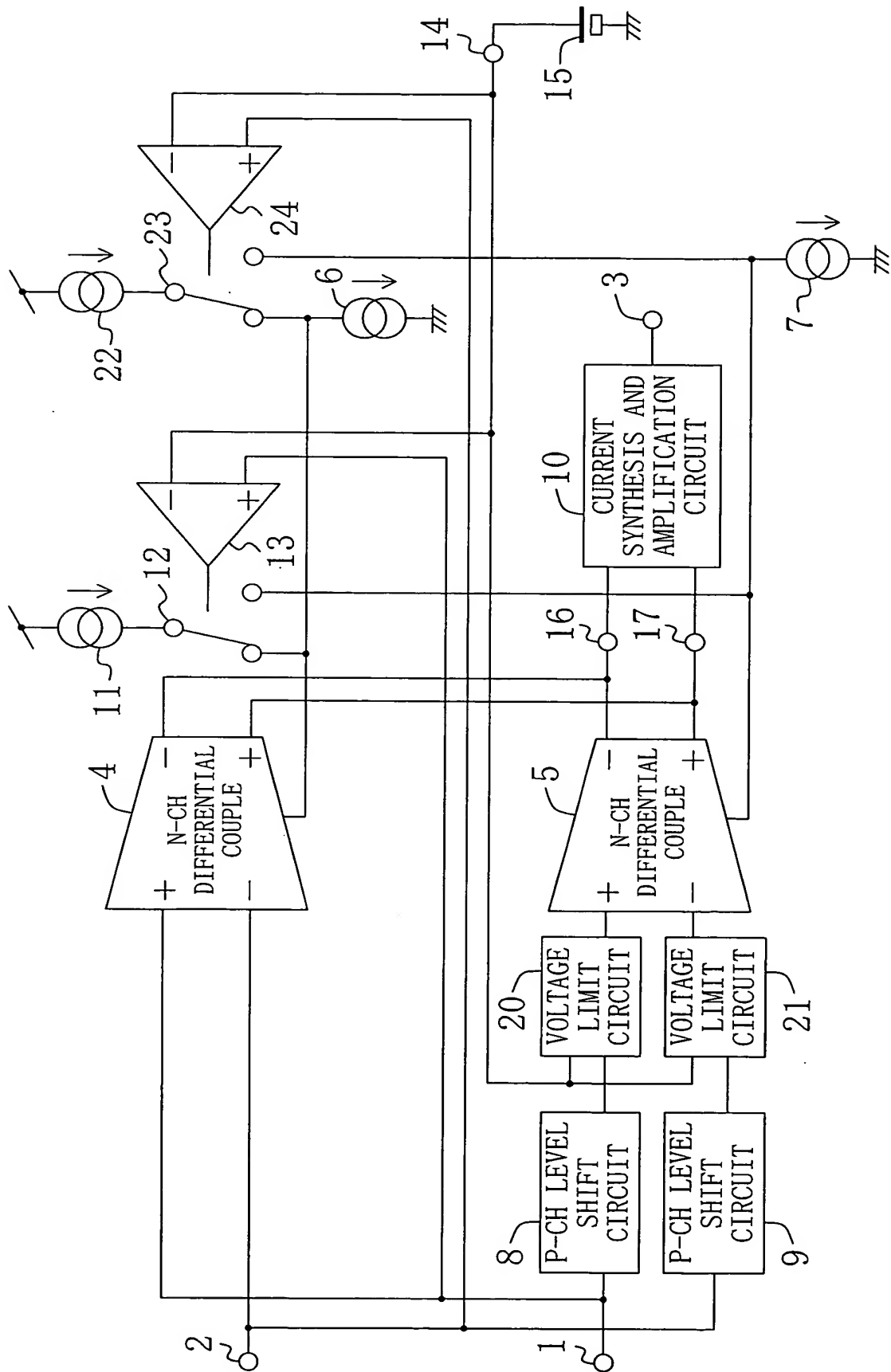


FIG. 18

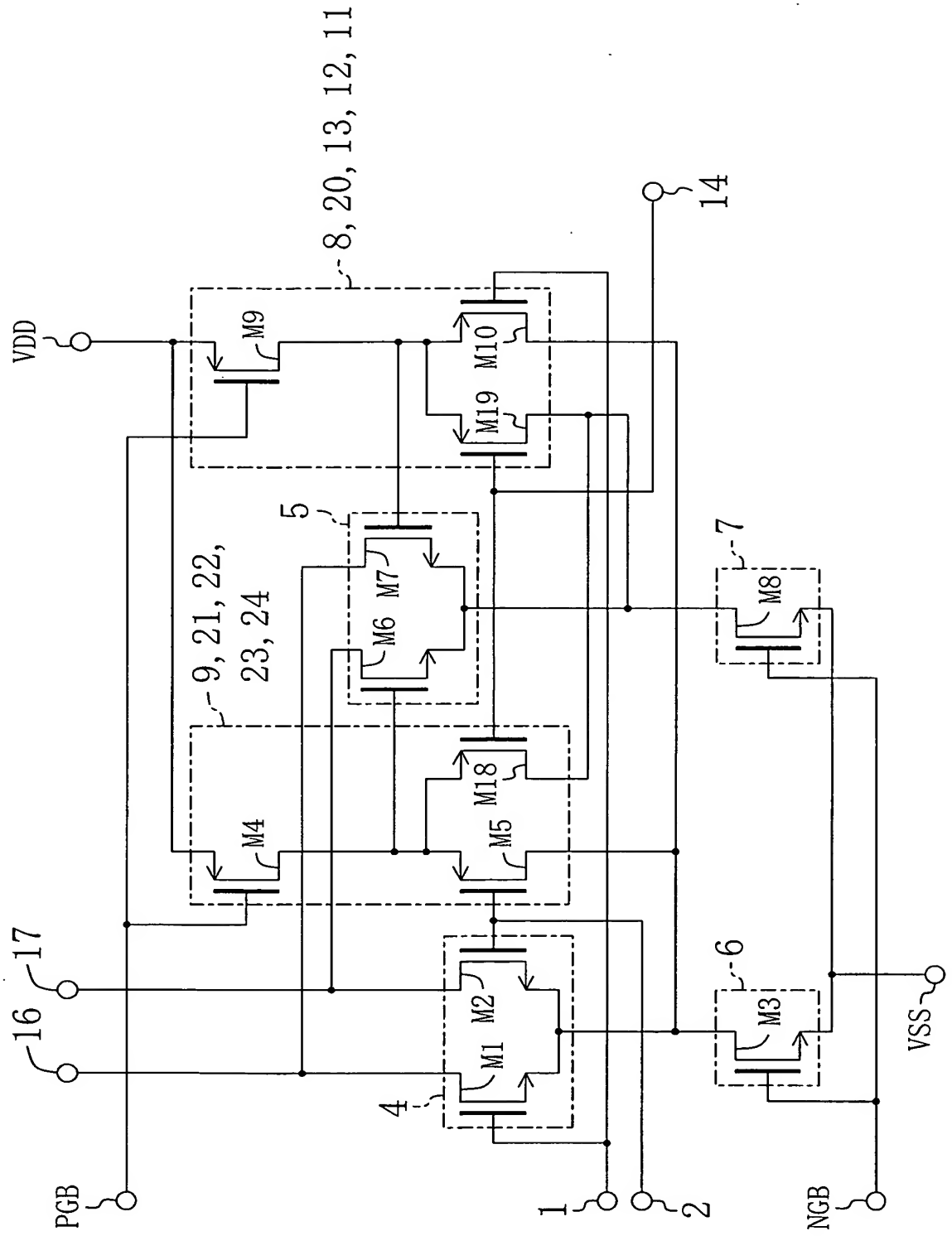


FIG. 19

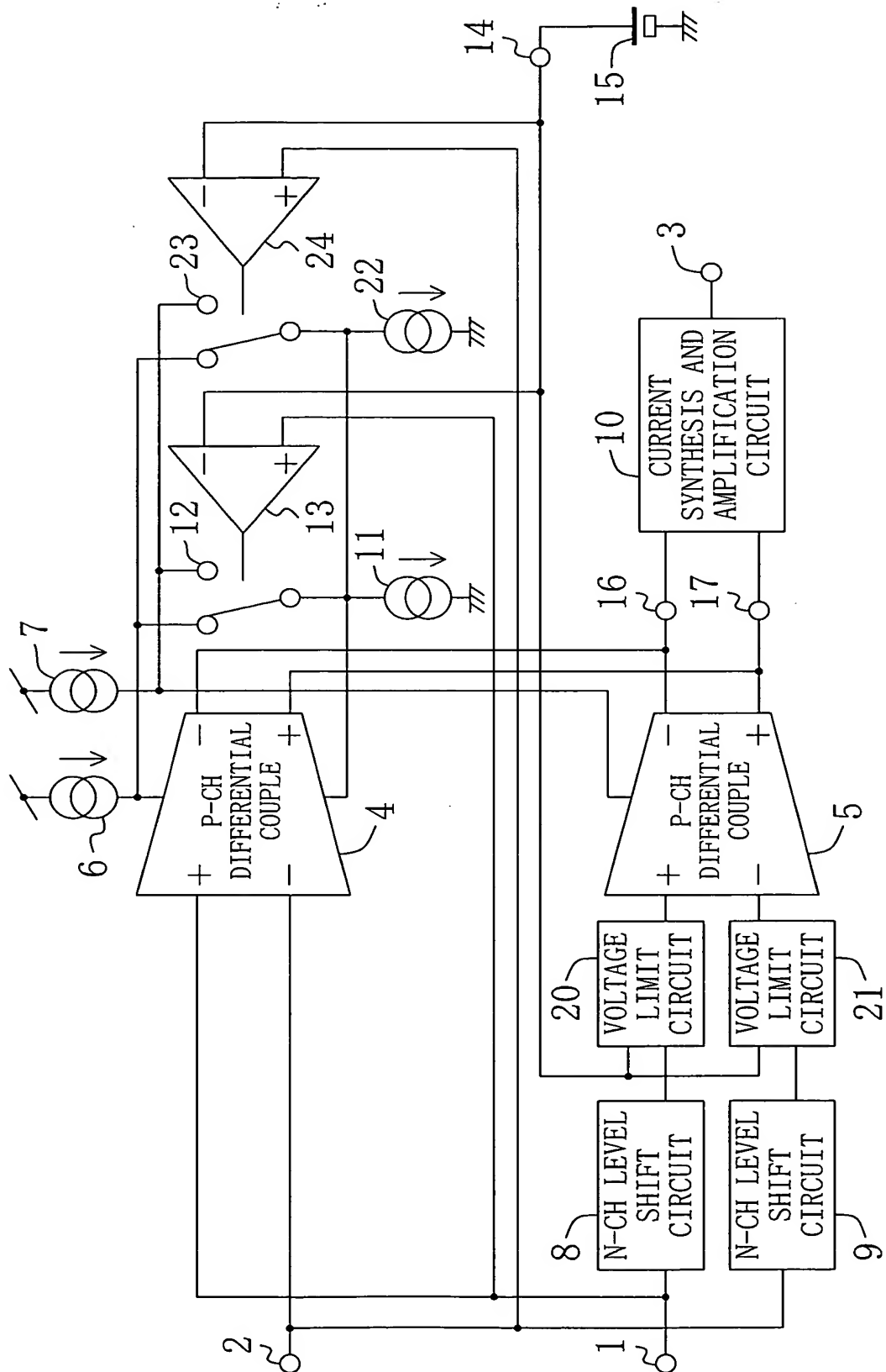
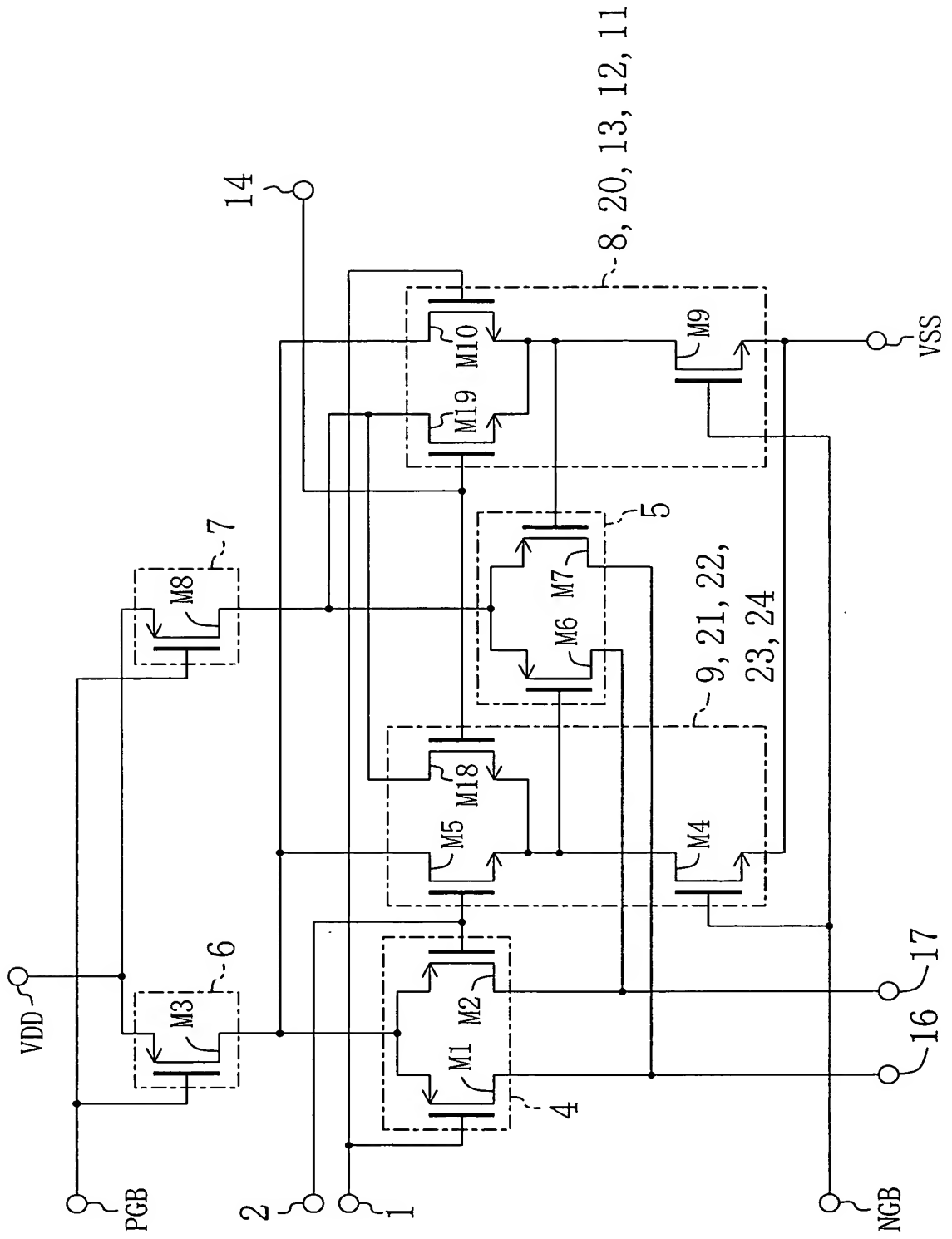


FIG. 20



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FIG. 21

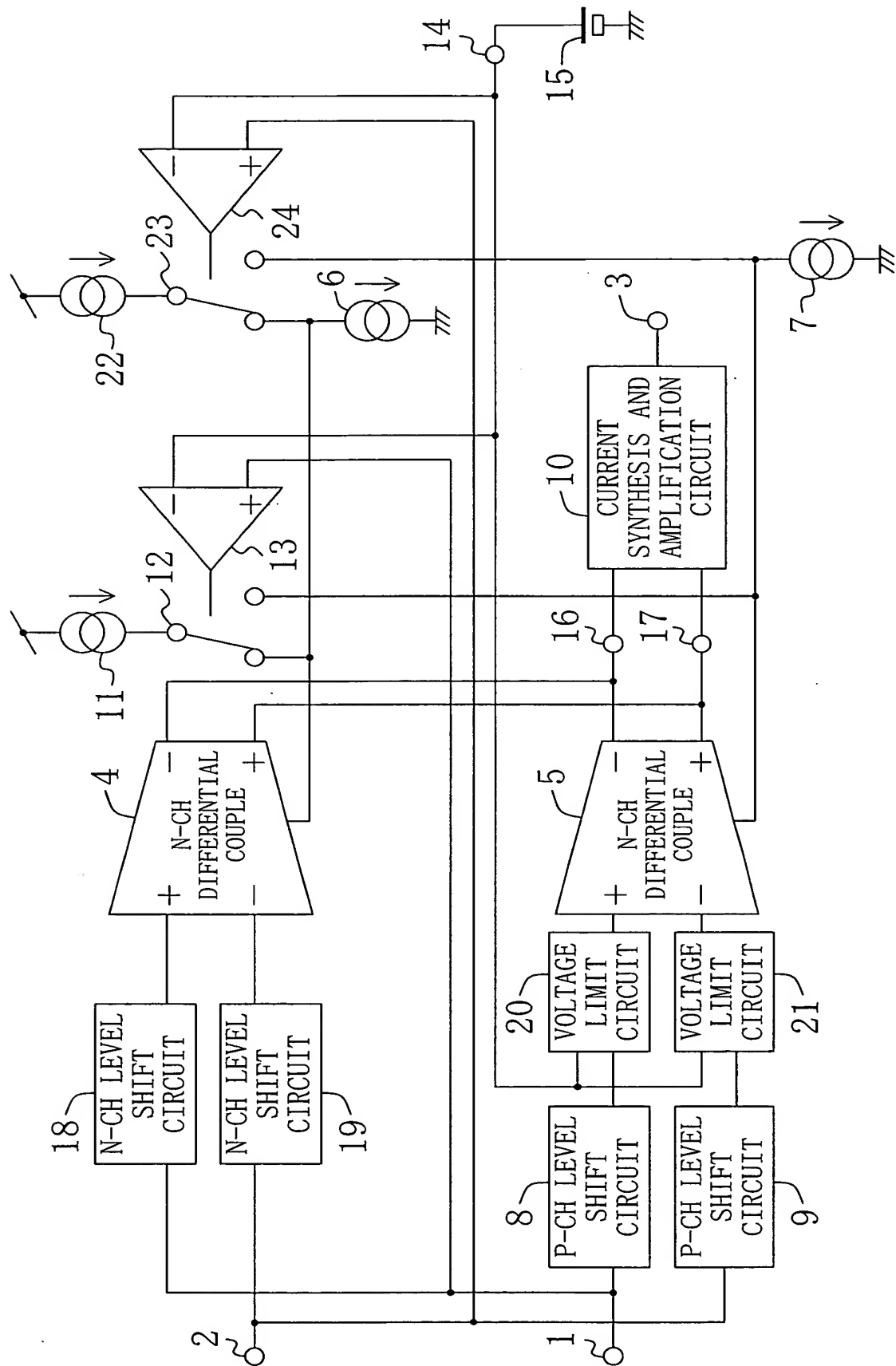


FIG. 22

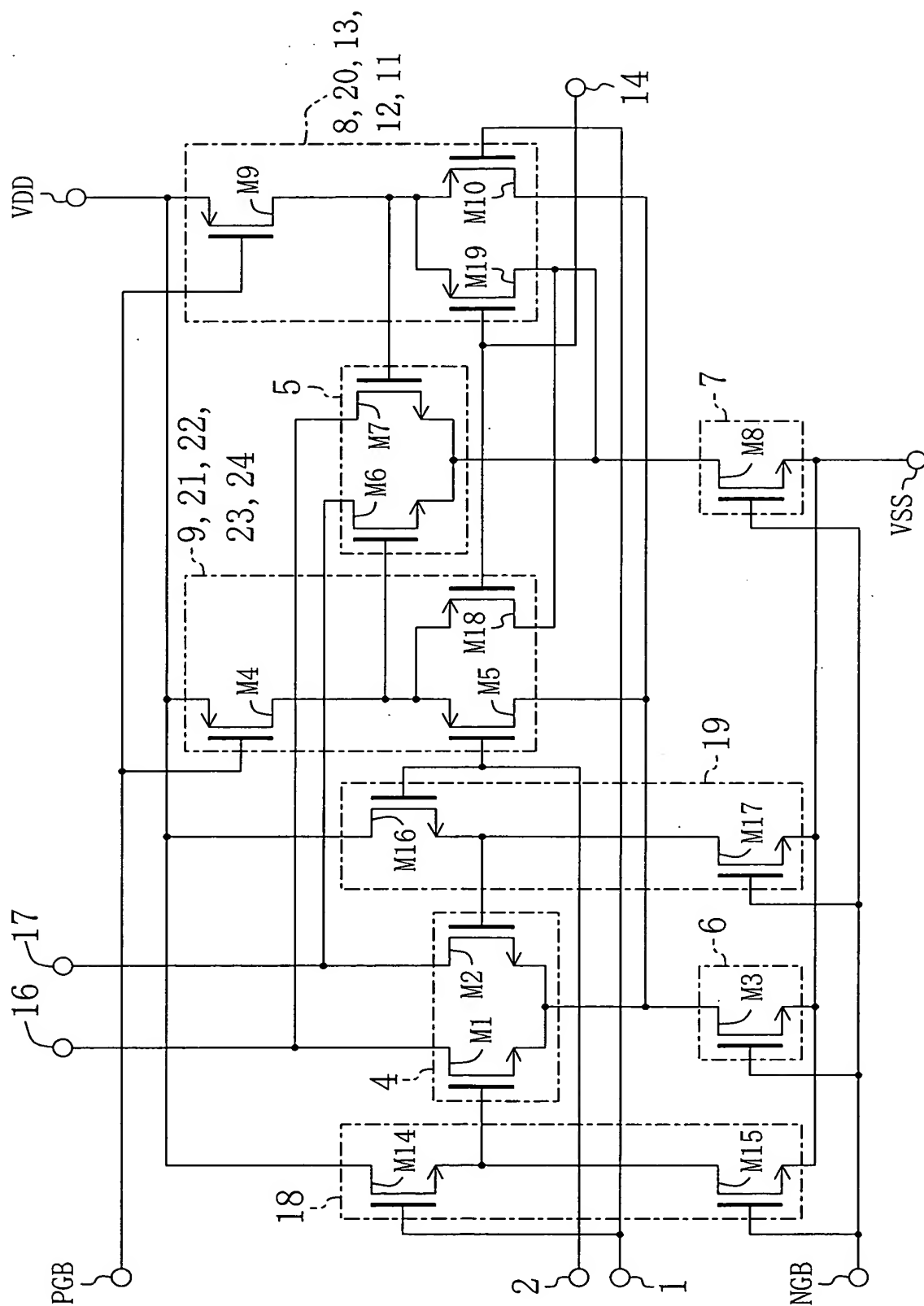


FIG. 23

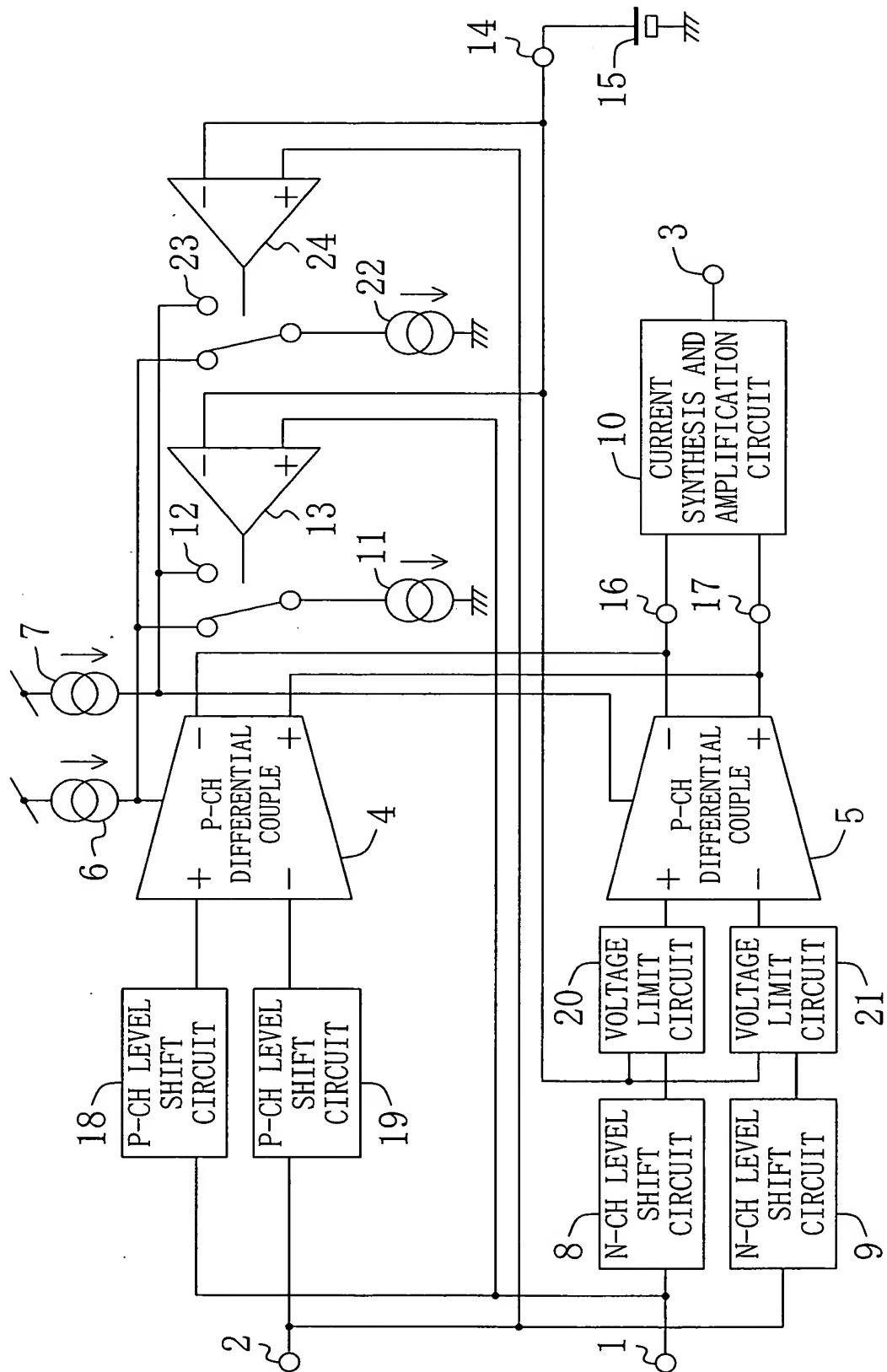


FIG. 24

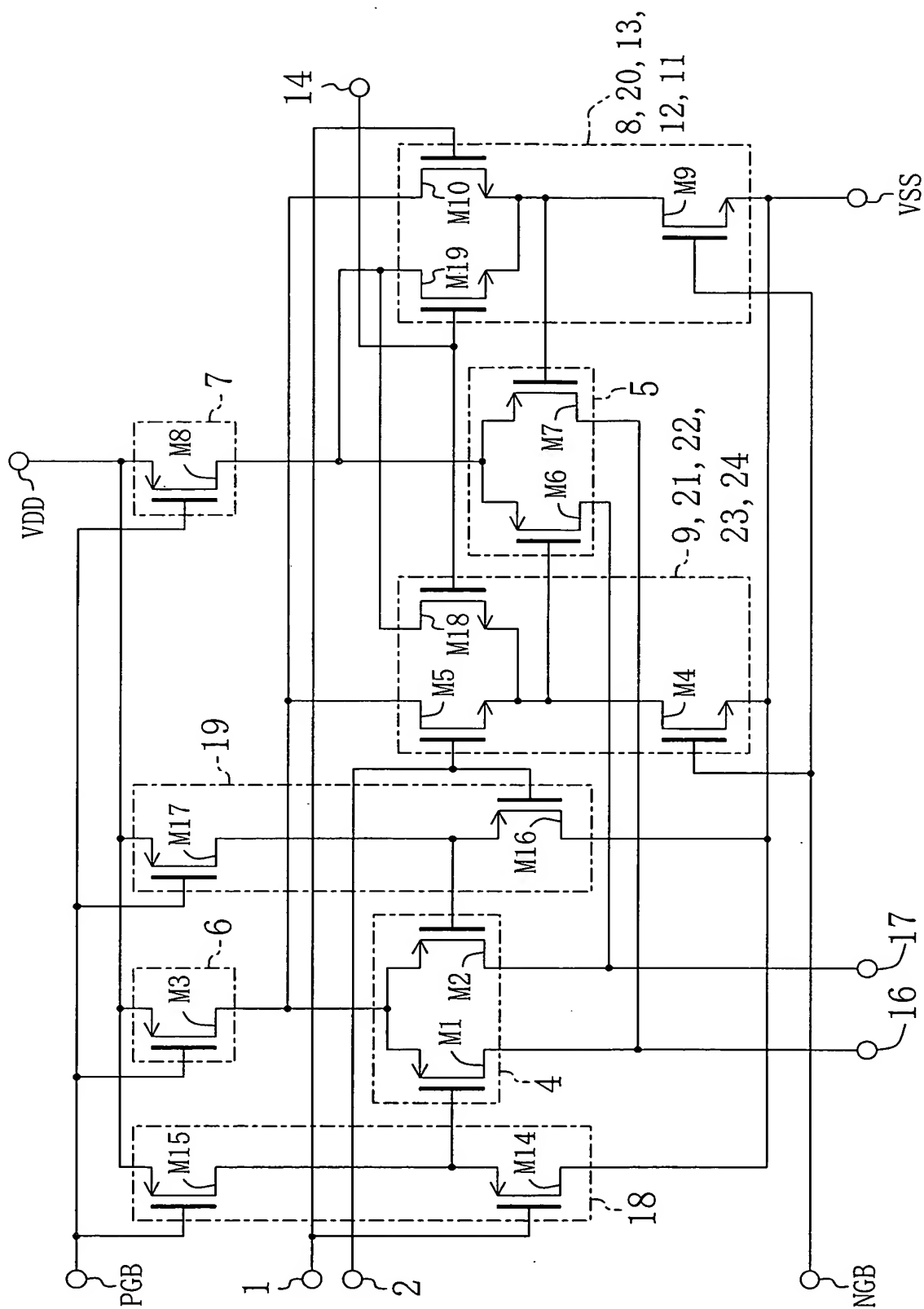




FIG. 25

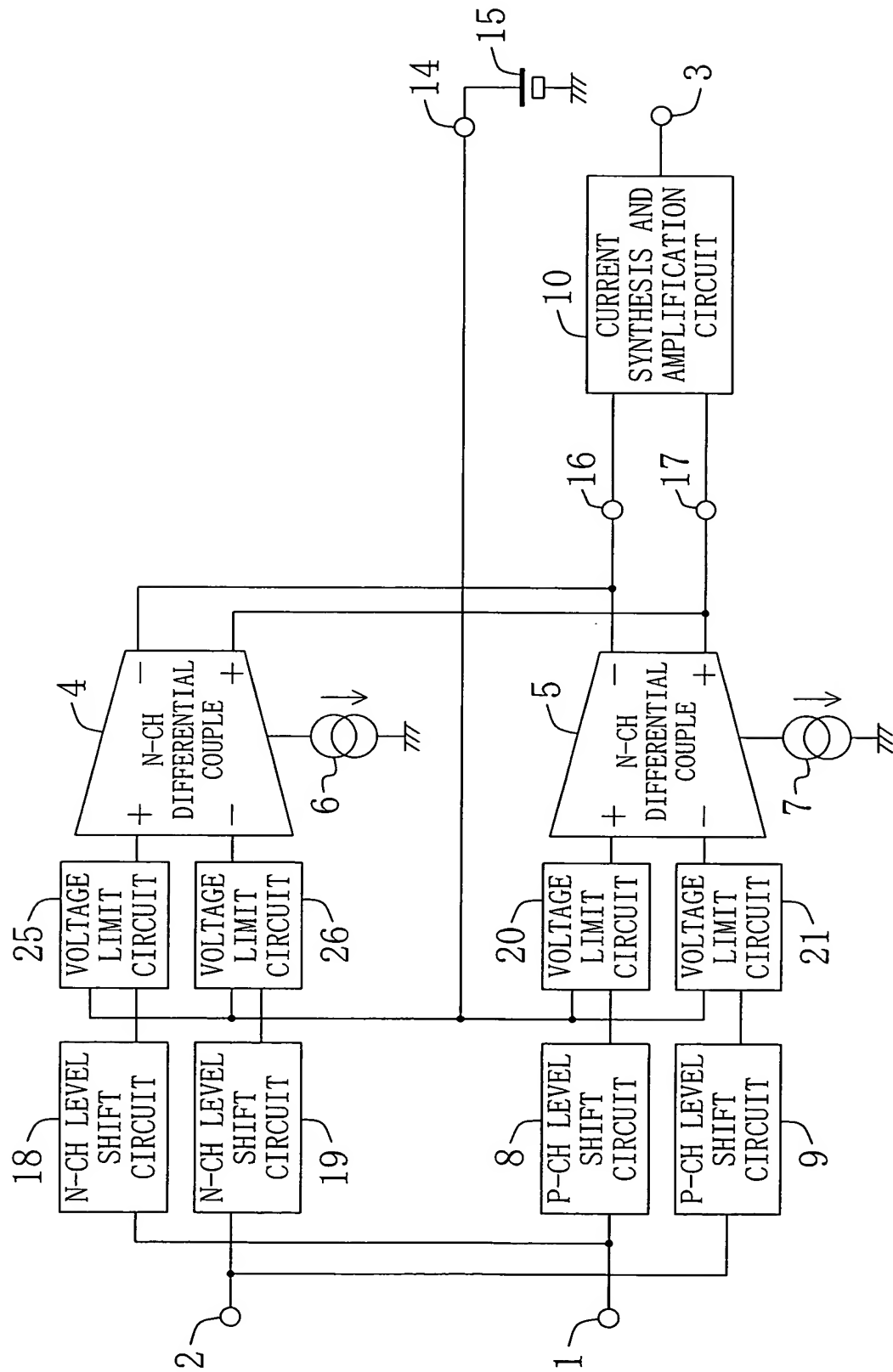


FIG. 26

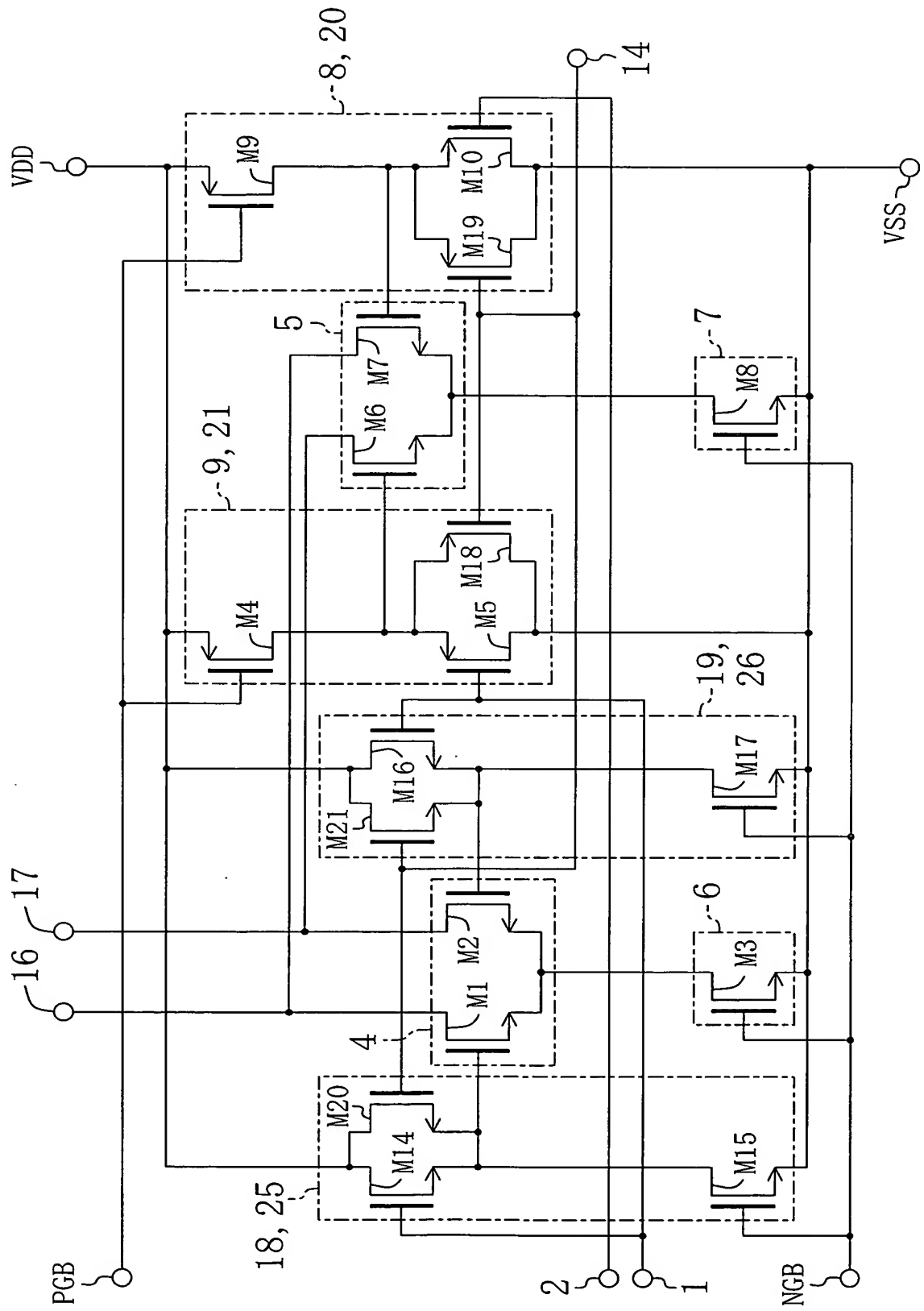


FIG. 27

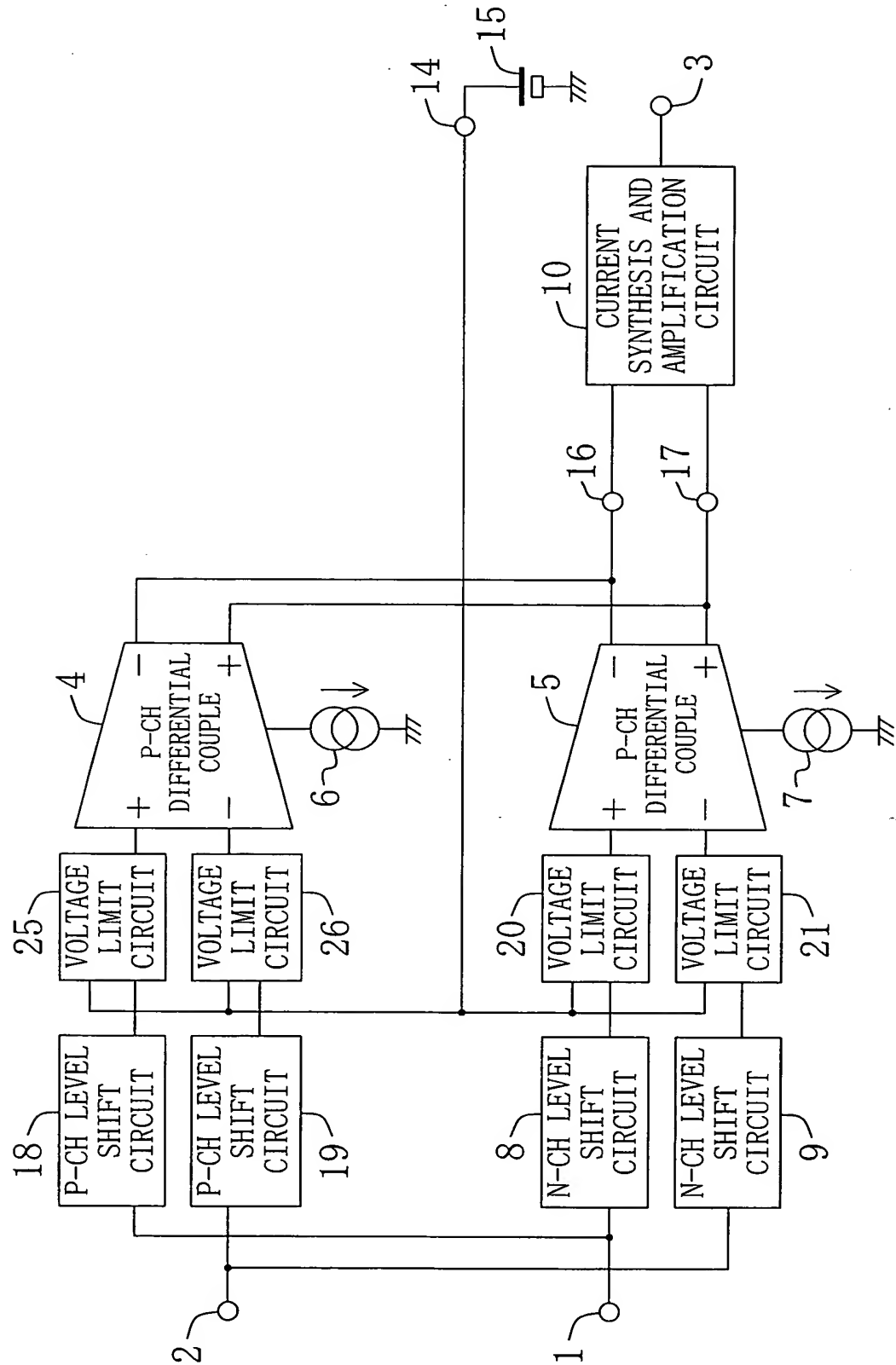


FIG. 28

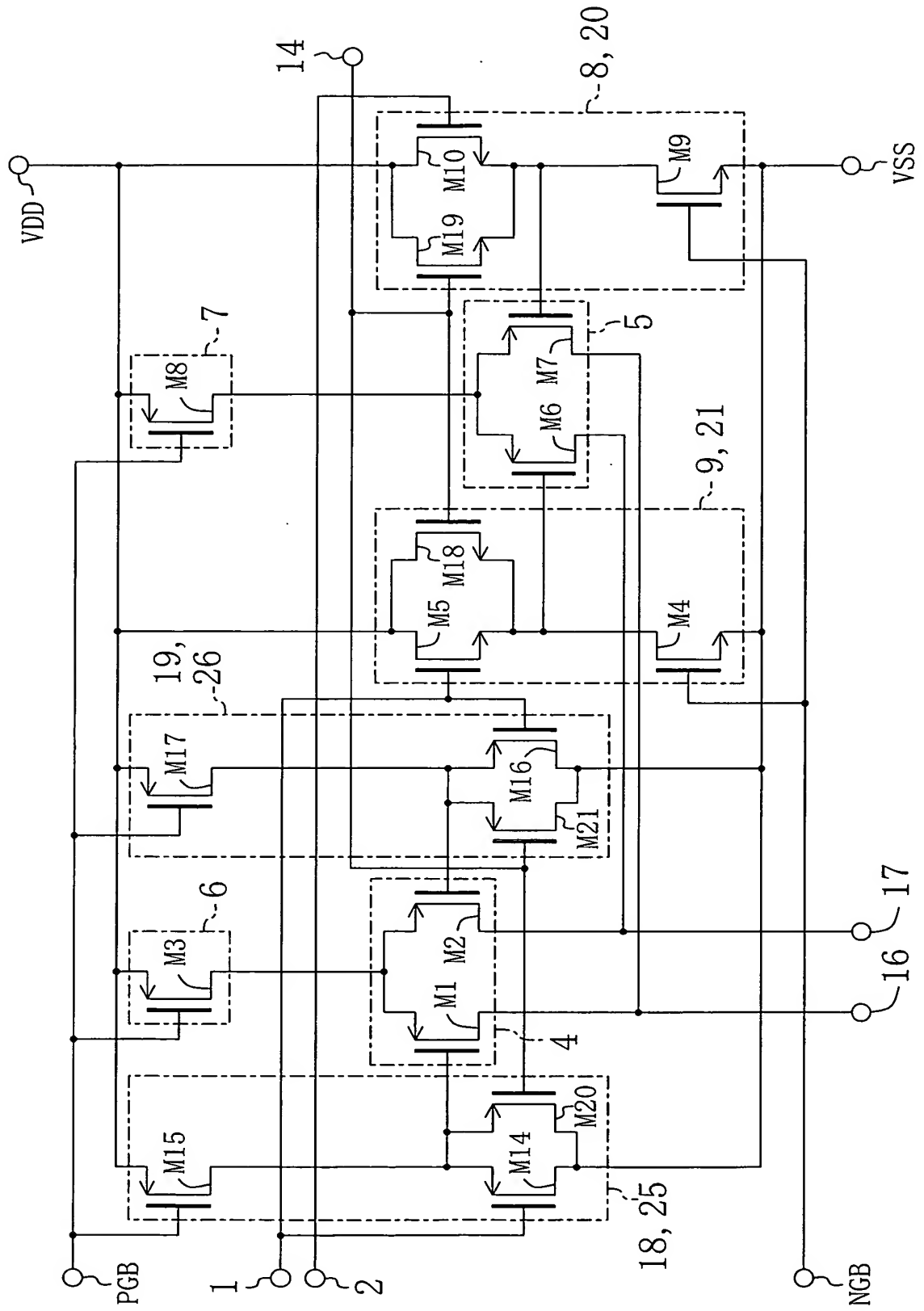


FIG. 29

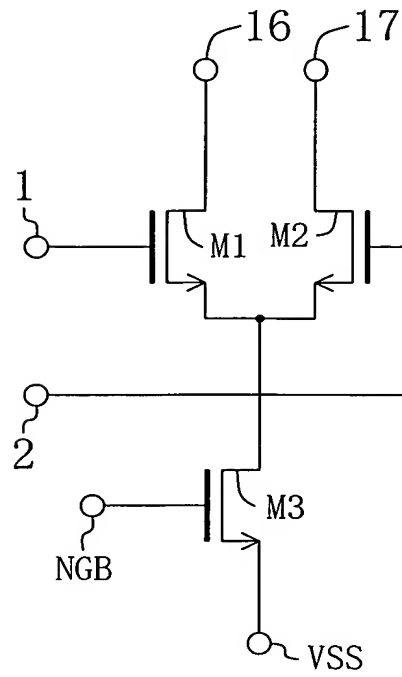


FIG. 30

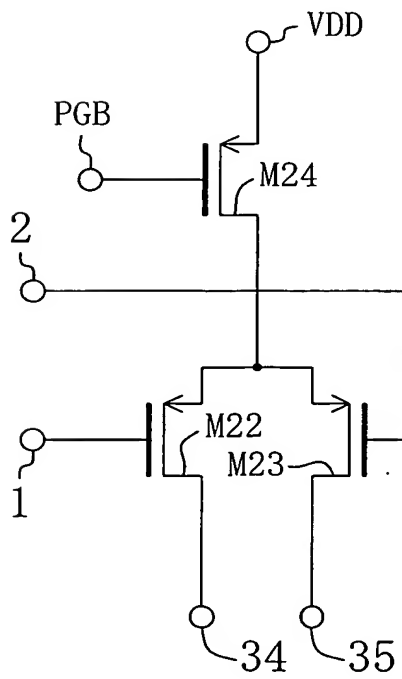


FIG. 31

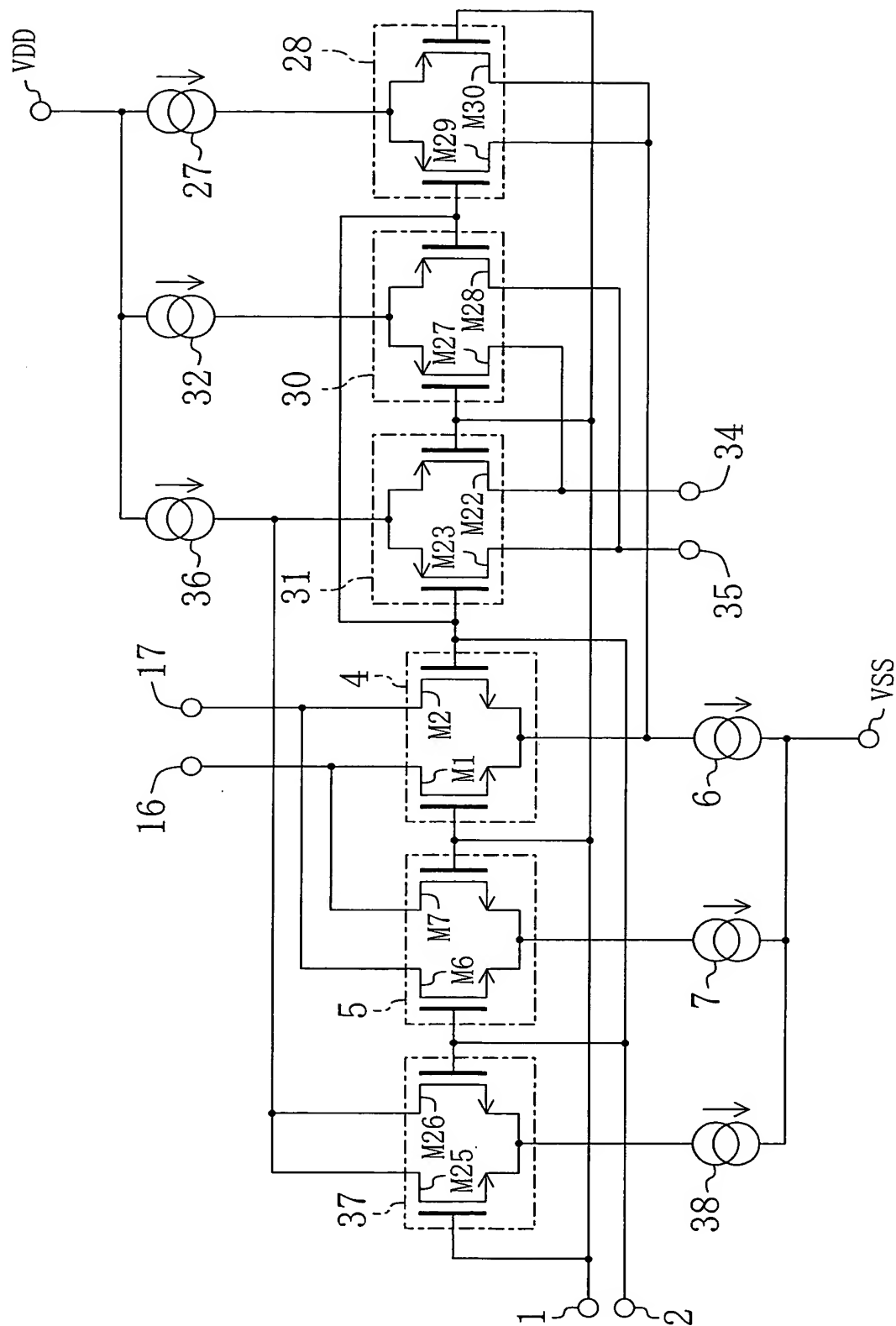


FIG. 32

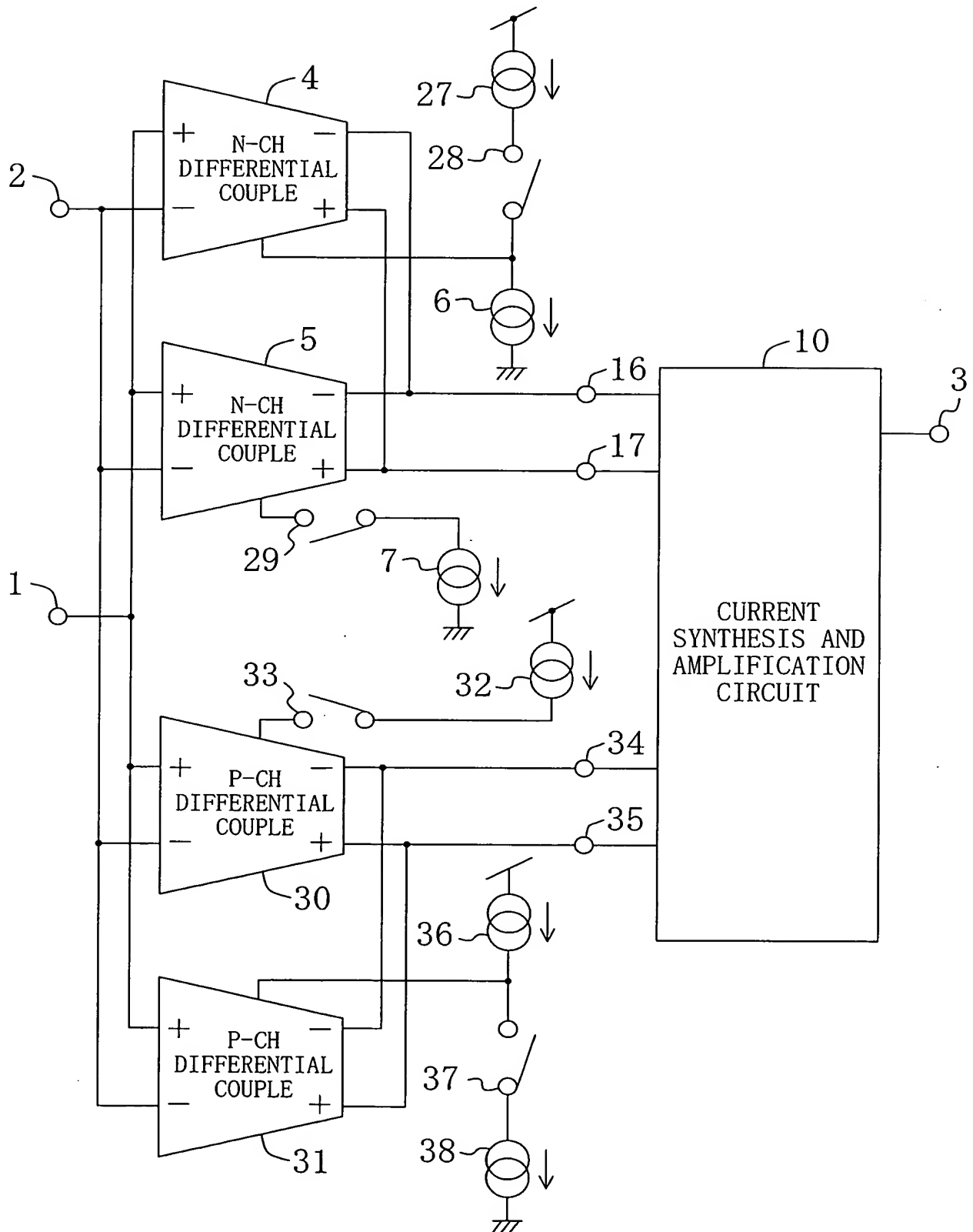


FIG. 33

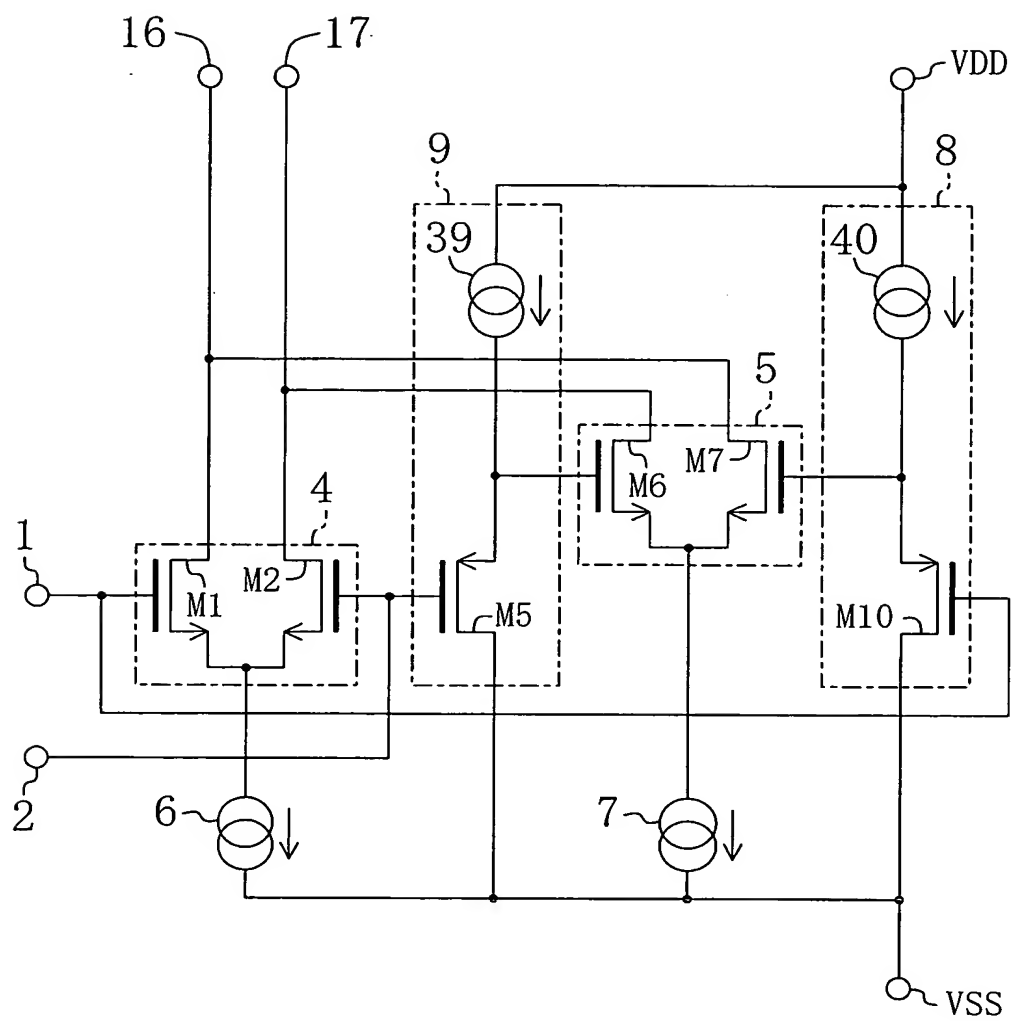




FIG. 34

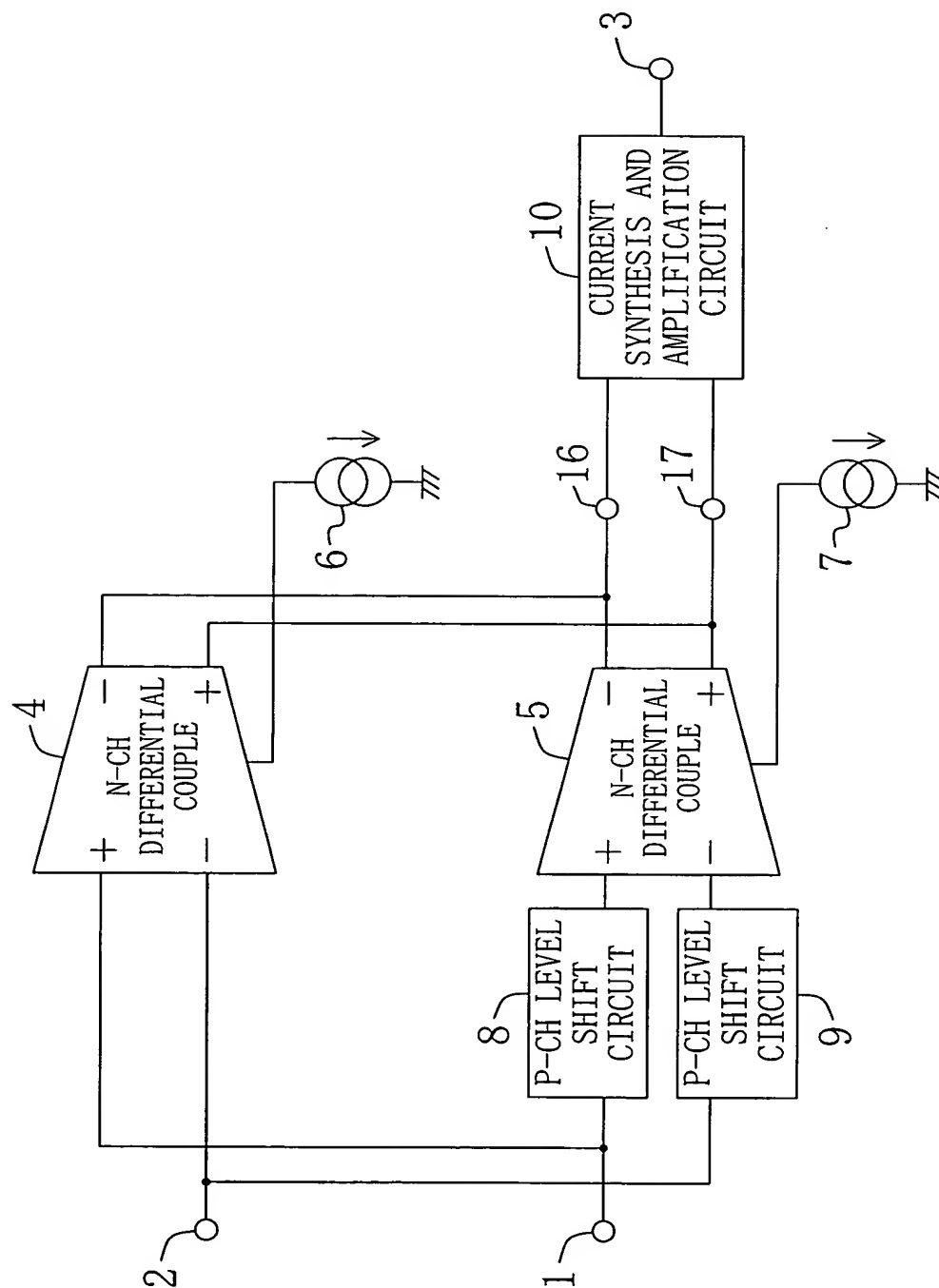


FIG. 35

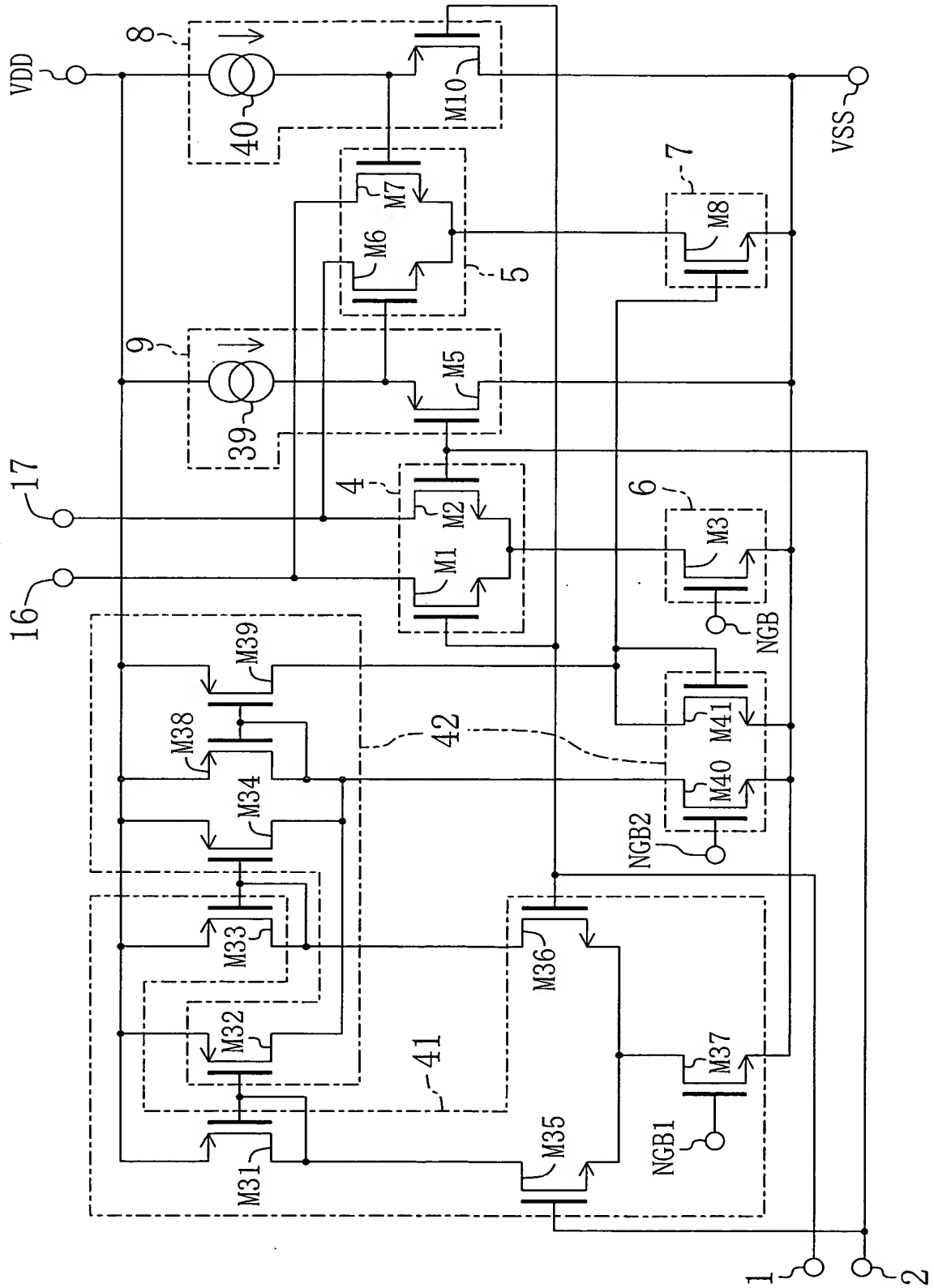


FIG. 36

